To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

32182 Group

Under Development

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Description

The 32182 Group is a 32-bit, single-chip RISC microcomputer with built-in flash memory, which was developed for use in general industrial and household equipment. To accomplish high-precision arithmetic operations, it incorporates a fully IEEE754 compliant, single-precision FPU.

This microcomputer contains a variety of peripheral functions ranging from 12-channel A-D converters, 37-channel multijunction timers, 10-channel DMACs, 4-channel serial I/Os, and 1-channel Real-time Debugger. Also included are 2-channel Full-CAN modules and JTAG (boundary scan facility). With the software necessary to run these numerous peripheral functions stored in its large-capacity flash memory, this microcomputer meets the needs of application systems for high functionality, high-performance arithmetic capability, and sophisticated control.

With lower power consumption and low noise characteristics also considered, these microcomputers are ideal for embedded equipment applications.

Features

M32R-FPU core

- Uses the M32R family RISC CPU core (M32R family common instruction set + single-precision FPU/extended instructions)
- Five-stage pipelined processing
- Sixteen 32-bit general-purpose registers
- 16-bit/32-bit instructions implemented
- DSP function instructions (multiply-Accumulate calculation using 56-bit accumulator)
- Built-in single-precision FPU (fully compliant with IEEE754 standard: four rounding modes, etc.)
- Bit manipulation extended instructions
- Built-in flash memory
- Built-in flash programming boot program
- Built-in RAM
- PLL clock generating circuit ..... Multiply by 8
- Oscillation stop detection function
- Maximum operating frequency of the CPU clock
  M32182F8VFP/M32182F3VFP
  ..... 64MHz (when operating at -40°C to +125°C)
  M32182F8TFP/M32182F3TFP
  ..... 80MHz (when operating at -40°C to +85°C)
- Single power supply: 5 V (± 0.5 V) or 3.3 V (± 0.3 V)

Table 1. Type Name List (32182 Group)

Type Name	RAM Size	ROM Size
M32182F8VFP/M32182F8TFP	64K bytes	1024K bytes
M32182F3VFP/M32182F3TFP	64K bytes	384K bytes

37-channel multijunction timers (MJT)

Multijunction timers are incorporated that support various purposes of use.

16-bit output related timers (TOP) ..... 11 channels
16-bit input/output related timers (TIO)..... 10 channels
16-bit input related timers (TMS) ..... 8 channels
32-bit input related timers (TML) ..... 8 channels

- Flexible configuration is possible through interconnection of timers.
- The internal DMAC and A-D converter can be started by a timer.

Real-time Debugger

- Includes dedicated clock-synchronized serial I/O that can read and write the contents of the internal RAM independently of the CPU.
- Can look up and update the data table in real time while the program is running.
- Can generate a dedicated interrupt based on RTD communication.

Abundant internal peripheral functions

In addition to the timers and real-time debugger, the microcomputer contains the following peripheral functions.

- DMAC ..... 10 channels
- A-D converters (Sample & hold function, Disconnection detector assist function, Injection current bypass circuit)
  ..... 12 channels 10-bit converter
- Serial I/O ..... 4 channels
- Interrupt controller: 23 interrupt sources, 8 priority levels
- Wait controller
- Full CAN (CAN Specification 2.0B active) ..... 2 channels
- Virtual-Flash emulation function ..... 4K bytes × 8 banks
- JTAG (boundary scan function, Mitsubishi original SDI debug function)
- Port input threshold level select function

Designed to operate at high temperatures

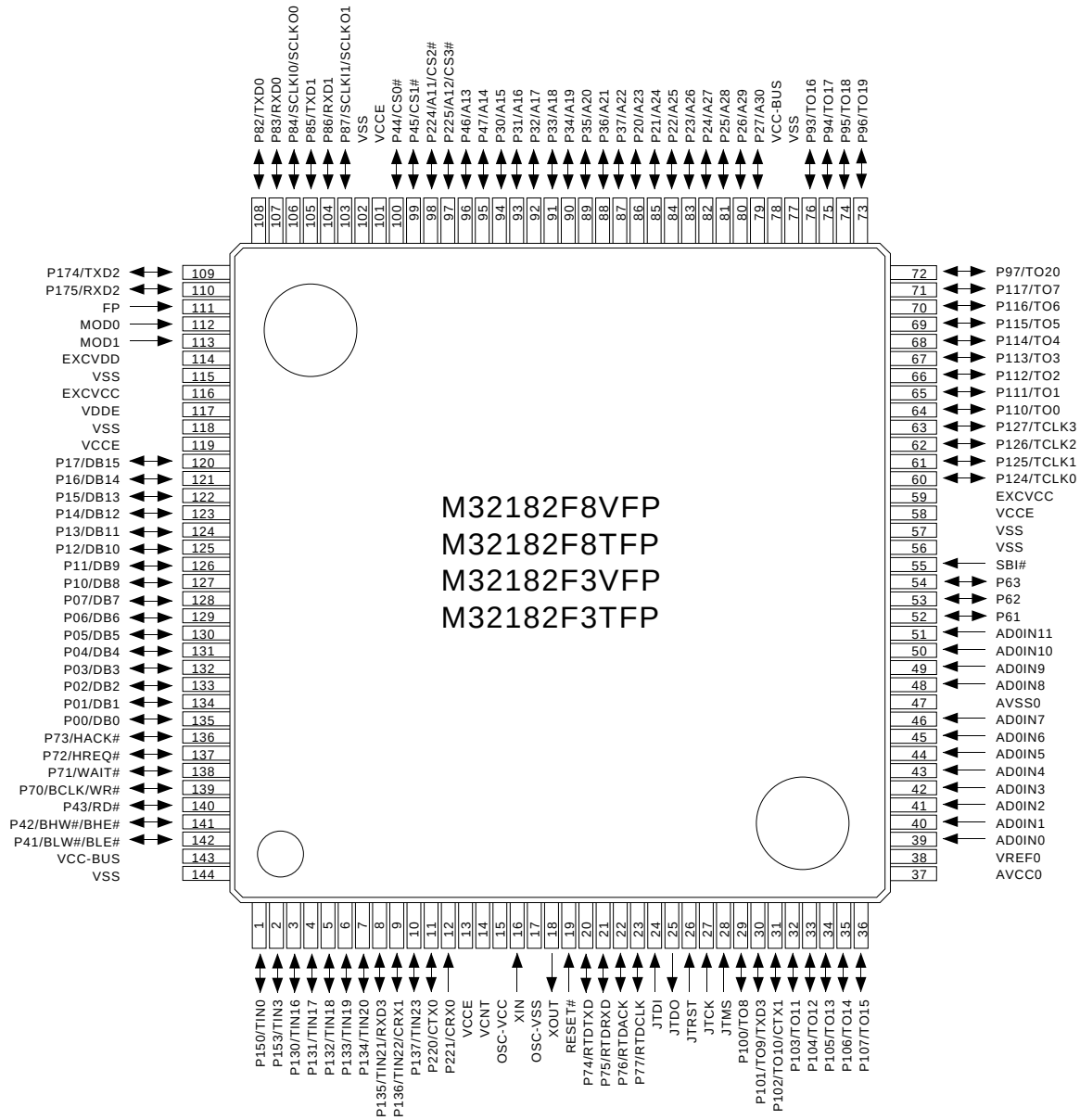
To meet the need for use at high temperatures, the microcomputer is designed to be able to operate in the temperature range of -40 to +125°C when CPU clock operating frequency = 64 MHz. When CPU clock operating frequency = 80 MHz, the microcomputer can be used in the temperature range of -40 to +85°C.

Note: • This does not guarantee continuous operation at 125°C. If you are considering use of the microcomputer at 125°C, please consult Mitsubishi.

Applications

Automobile equipment control (e.g., Engine, ABS, and AT), industrial equipment system control, and high-function OA equipment (e.g., PPC)

Pin Assignment (top view)



Package 144P6Q-A

Note: • It is shown that the pin (signal) with which "#" sticks to the last of a pin name (signal name) is "L" active pin (signal).

Figure 1. Pin Layout Diagram

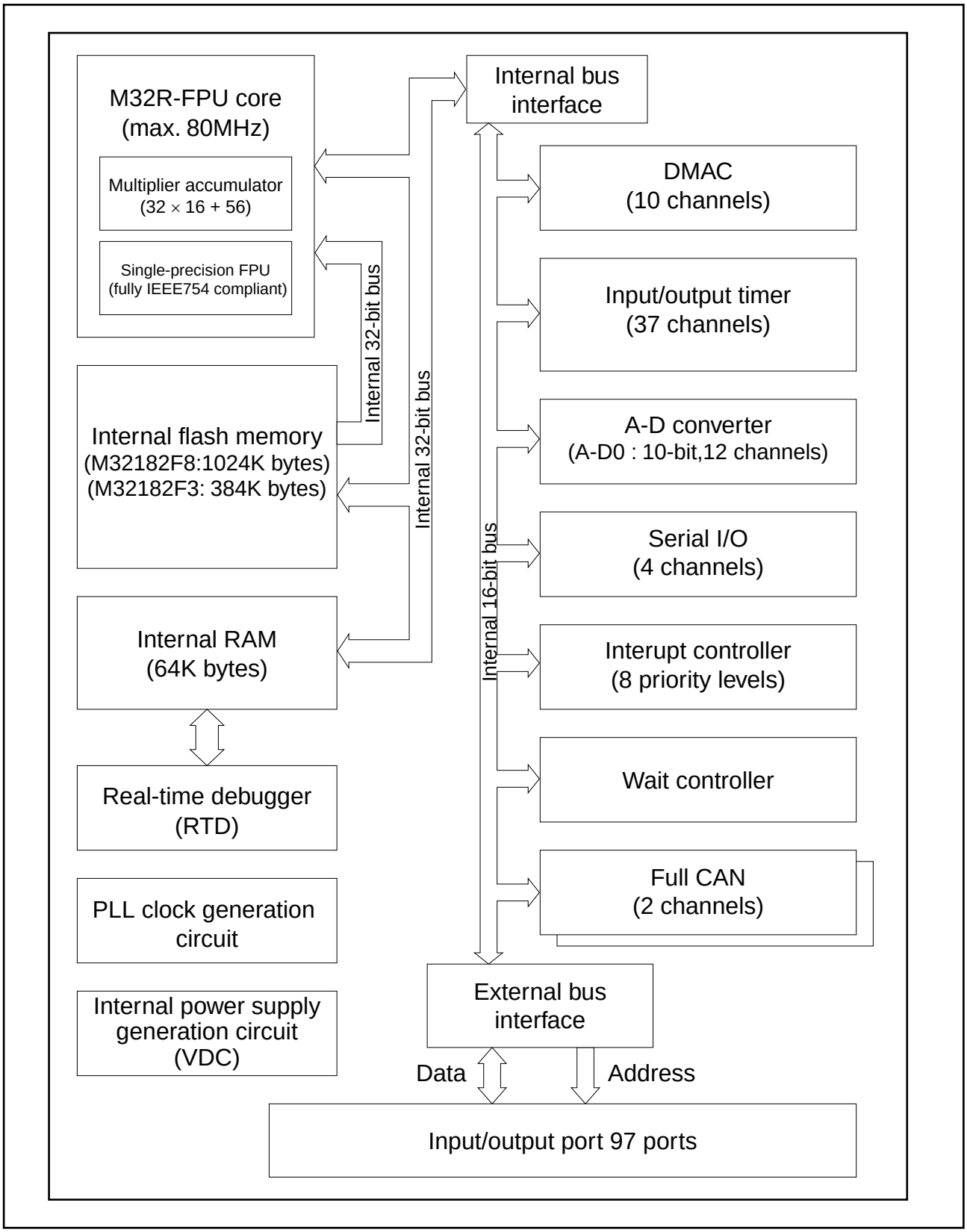


Figure 2. Block diagram

Table 2. Outline Performance (1/2)

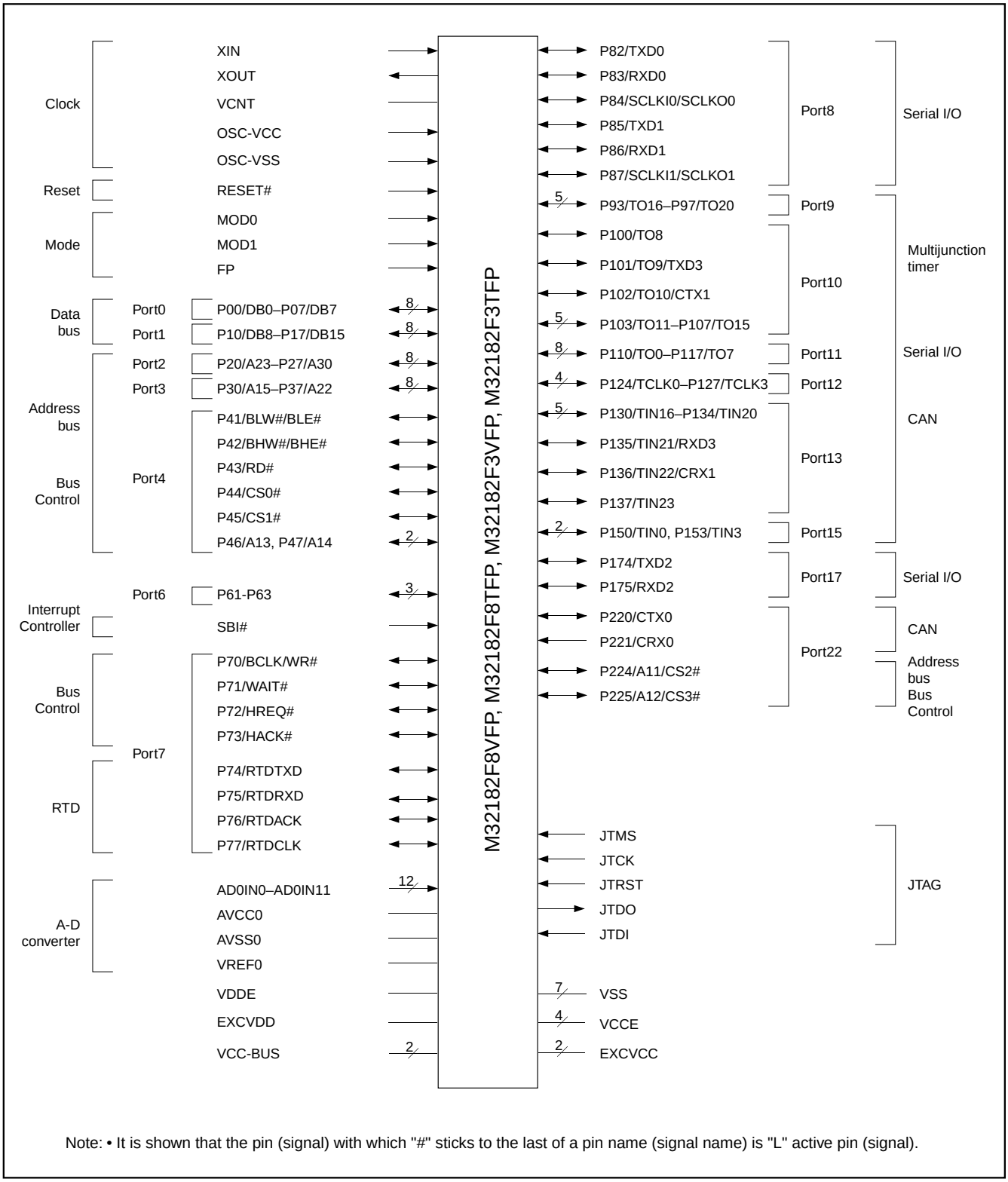
Functional Block	Features
M32R-FPU core	M32R family CPU core, internally configured in 32-bit Built-in multiplier-accumulator (32 × 16 + 56) Basic bus cycle: 15.625 ns (CPU clock frequency at 64 MHz, Internal peripheral clock frequency at 16MHz) : 12.5 ns (CPU clock frequency at 80 MHz, Internal peripheral clock frequency at 20MHz) Logical address space: 4G bytes, linear General-purpose register: 32-bit register × 16,Control register: 32-bit register × 6 Accumulator: 56-bit
External data bus	16-bit data bus
Instruction set	16-bit/32-bit instruction formats 100 discrete instructions in six addressing modes
Internal flash memory	M32182F8VFP/M32182F8TFP: 1024K bytes M32182F3VFP/M32182F3TFP: 384K bytes Rewrite durability: 100 times
Internal RAM	64K bytes
DMAC	10 channels (DMA transfers between internal peripheral I/Os, between internal peripheral I/O and internal RAM, and between internal RAMs) Channels can be cascaded and can operate in combination with internal peripheral I/O
Multijunction timer	37 channels of multijunction timers. TOP : 16-bit output related timer, 11 channels (single-shot, delayed single-shot, and continuous) TIO : 16-bit input/output related timer, 10 channels (measure clear, measure free-run, noise processing input, PWM, single-shot, delayed single-shot, continuous output) TMS : 16-bit input related timer, 8 channels (measure input) TML : 32-bit input related timer, 8 channels (measure input) Flexible timer configuration is possible through interconnection of channels using the clock bus or event bus.
A-D converter	10-bit multifunction A-D converters • Input 12 channels • Scan-based conversion can be switched between N (N = 1–12) channels • Capable of interrupt conversion during scan • 8-bit/10-bit readout function • Sample & hold function • Disconnection detector assist function • Injection current bypass circuit
Serial I/O	4 channels (The serial I/Os can be set for synchronous serial I/O or UART. SIO2, SIO3 are UART mode only)
Real-time Debugger (RTD)	1-channels dedicated clock-synchronized serial • Entire area of internal RAM Can access the internal RAM for read/rewrite from outside independently of the CPU, and also generate an exclusive-use interrupt.
Interrupt controller	Controls interrupts from internal peripheral I/Os (Priority can be set to one of 8 levels including interrupt disabled)
Wait controller	Controls wait when accessing external extended area (Chip selects for four external extended areas each can have access extended for 0–7 wait cycles plus WAIT# signal entered from external source) (Note 1)
CAN	Two channels, each having 16-channel message slots
JTAG	Boundary-Scan function, Built-in SDI debugger function in MITSUBISHI
Clock	M32182F8VFP, M32182F3VFP: CPU clock: maximum 64 MHz (for CPU, internal ROM, and internal RAM access) Internal peripheral clock (BCLK): maximum 16 MHz (for peripheral module access) External input clock (XIN): maximum 8.0 MHz, built-in ×8 PLL circuit M32182F8TFP, M32182F3TFP: CPU clock: maximum 80 MHz (for CPU, internal ROM, and internal RAM access) Internal peripheral clock (BCLK): maximum 20 MHz (for peripheral module access) External input clock (XIN): maximum 10.0 MHz, built-in ×8 PLL circuit

Table 2. Outline Performance (2/2)

Functional Block	Features
Power Supply Voltage	5V (± 0.5V) or 3.3V (± 0.3V) [T.B.D]: single power supply voltage (The internal logic operates with 2.5V, however)
Operating temperature range (Note 2)	M32182F8VFP, M32182F3VFP: -40 to +125°C (CPU clock 64MHz, internal peripheral clock 16MHz) M32182F8TFP, M32182F8TFP: -40 to +85°C (CPU clock 80MHz, internal peripheral clock 20MHz)
Package	0.5mm pitches / 144-pin LQFP package (144P6Q-A)

Note 1: Wait Cycle by the external WAIT# input is not received when 0wait is selected. Moreover, as for all idol setup after the wait / strike robe / recovery / lead of CS block, only operation by "nothing" setup is guaranteed when 0wait is selected.

Note 2: This does not mean that the microcomputer is guaranteed for continuous operation at 125°C. If 125°C applications are desired, please consult Mitsubishi.



Note: • It is shown that the pin (signal) with which "#" sticks to the last of a pin name (signal name) is "L" active pin (signal).

Figure 3. Pin Function Diagram

Table 3. Description of Pin Function (1/3)

Type	Pin	Name	Input/Output	Function
Power Supply	VCCE	Power supply	-	Power supply (5.0V ± 0.5V or 3.3V ± 0.3V).
	EXCVCC	External capacitance connect	-	External capacitance connecting pin.
	VCC-BUS	Bus power supply	-	Power supply for the bus control pins (5.0V ± 0.5V or 3.3V ± 0.3V).
	VDDE	RAM power supply	-	Internal RAM backup power supply (5.0V ± 0.5V or 3.3V ± 0.3V).
	EXCVDD	External capacitance connect	-	Backup power supply for the internal RAM, external capacitance connecting pin.
	VSS	Ground	-	Connect all VSS pins to ground (GND).
Clock	XIN	Clock input	Input	Clock input/output pins. These pins contain a PLL-based frequency multiply-by-8, so input the clock whose frequency is 1/8 the operating frequency. (XIN input = 10 MHz when CPU clock operates at 80 MHz)
	XOUT	Clock output	Output	
	BCLK	System clock	Output	Outputs a clock twice the externally sourced clock frequency, XIN (when the internal CPU memory clock is 80 MHz, BCLK output = 20 MHz). Use this output when external sync design is desired.
	OSC-VCC	Clock power supply	-	Power supply to the PLL circuit. Connect OSC-VCC to the power supply
	OSC-VSS	Clock ground	-	Connect OSC-VSS to ground.
	VCNT	PLL control	-	This pin controls the PLL circuit. Connect a resistor and capacitor to this pin.
Reset	RESET#	Reset	Input	This pin resets the internal circuits.
Mode	MOD0, MOD1	Mode	Input	These pins set an operation mode. MOD0 / MOD1 / Mode 0 / 0 / Single-chip mode 0 / 1 / Expanded external mode 1 / 0 / Processor mode (Boot mode) (Note 1) 1 / 1 / (Do not select) Note: In boot mode, the FP pin must be at the high level.
Flash-only	FP	Flash Protect	Input	This pin protects the flash memory against E/W in hardware.
Address Bus	A11–A30	Address bus	Output	To allow four blocks of up to 2 MB memory space each to be added externally, 20-bit address (A11–A30) is provided. A31 is not output.
Data bus	DB0–DB15	Data bus	Input/output	This is a 16-bit data bus connecting to an external device. During write cycle, the microcomputer outputs BHW# or BLW# to indicate the valid byte write position of the 16-bit data bus. During read cycle, the microcomputer always reads the full 16-bit data bus. Transferred to the internal circuit of the M32R, however, is the data at only the valid byte position.
Bus Control	CS0#–CS3#	Chip select	Output	Chip select signals for external devices.
	RD#	Read	Output	This signal is output when reading external devices.
	WR#	Write	Output	This signal is output when writing external devices.
	BHW#	Byte High Write	Output	Indicates the byte positions to which valid are transferred when writing to external devices. BHW#/ BHE# and BLW#/ BLE# correspond to the upper address side (DB0–DB7 effective) and the lower address side (DB8–DB15 effective), respectively.
	BLW#	Byte Low Write	Output	
	BHE#	Byte High Enable	Output	For external device access, it indicates that the upper byte data (DB0–DB7) is valid.
	BLE#	Byte Low Enable	Output	For external device access, it indicates that the lower byte data (DB8–DB15) is valid.
	WAIT#	Wait	Input	If WAIT# input is low when the M32R accesses external devices, the wait cycle extended.
	HREQ#	Hold request	Input	This pin is used by an external device to request control of the external bus. The M32R goes to a hold state when HREQ# input is pulled low.
	HACK#	Hold acknowledge	Output	This signal indicates to the external device that the M32R has entered a hold state and relinquished control of the external bus.

Note 1: In boot mode, the FP pin must be at the high level.

Table 3. Description of Pin Function (2/3)

Type	Pin	Name	Input/Output	Function
Multijunction timer	TIN0, TIN3 TIN16–TIN23	Timer input	Input	Input pin for multijunction timer
	TO0 –TO20	Timer output	Output	Output pin for multijunction timer
	TCLK0 –TCLK3	Timer clock	Input	Clock input pin for multijunction timers.
A-D converter	AVCC0	Analog power supply	-	AVCC0 is the power supply for the A-D0 converter. Connect AVCC0 to the power supply rail.
	AVSS0	Analog ground	-	AVSS0 is the analog ground for the A-D0 converters. Connect AVSS0 to ground.
	AD0IN0 –AD0IN11	Analog input	Input	16-channel analog input pins for the A-D0 converter in the first block.
	VREF0	Reference voltage input	Input	VREF0 is the reference voltage input pin for the A-D0 converter.
Interrupt controller	SBI#	System break interrupt	Input	System break interrupt (SBI) input pin of the interrupt controller
Serial I/O	SCLKI0/ SCLKO0	UART transmit/receive clock output or CSIO transmit/receive clock input/output	Input/output	When Channel 0 is in UART mode: Clock output derived from BRG output by dividing it by 2 When Channel 0 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	SCLKI1/ SCLKO1	UART transmit/receive clock output or CSIO transmit/receive clock input/output	Input/output	When Channel 1 is in UART mode: Clock output derived from BRG output by dividing it by 2 When Channel 1 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	TXD0	Transmit data	Output	Transmit data output pin of serial I/O channel 0
	RXD0	Receive data	Input	Receive data input pin of serial I/O channel 0
	TXD1	Transmit data	Output	Transmit data output pin of serial I/O channel 1
	RXD1	Receive data	Input	Receive data input pin of serial I/O channel 1
	TXD2	Transmit data	Output	Transmit data output pin of serial I/O channel 2
	RXD2	Receive data	Input	Receive data input pin of serial I/O channel 2
	TXD3	Transmit data	Output	Transmit data output pin of serial I/O channel 3
	RXD3	Receive data	Input	Receive data input pin of serial I/O channel 3

Table 3. Description of Pin Function (3/3)

Type	Pin	Name	Input/Output	Function
Real-time Debugger	RTDTXD	Transmit data	Output	Serial data output pin of the Real-time Debugger
	RTDRXD	Receive data	Input	Serial data input pin of the Real-time Debugger
	RTDCLK	Clock input	Input	Serial data transmit/receive clock input pin of the Real-time Debugger
	RTDACK	Acknowledge	Output	This pin outputs a low pulse synchronously with the Real-time Debugger's first clock of serial data output word. The low pulse width indicates the type of the command/data the Real-time Debugger has received.
CAN	CTX0, CTX1	Transmit data	Output	Data output pin from CAN module.
	CRX0, CRX1	Receive data	Input	Data input pin to CAN module.
JTAG	JTMS	Test mode	Input	Test select input for controlling the test circuit's state transition
	JTCK	Clock	Input	Clock input to the debugger module and test circuit.
	JTRST	Test reset	Input	Test reset input for initializing the test circuit asynchronously.
	JTDO	Serial output	Output	Serial output of test instruction code or test data.
	JTDI	Serial input	Input	Serial input of test instruction code or test data.
Input/output Port (Note 1)	P00–P07	Input/output port 0	Input/output	Programmable input/output port.
	P10–P17	Input/output port 1	Input/output	Programmable input/output port.
	P20–P27	Input/output port 2	Input/output	Programmable input/output port.
	P30–P37	Input/output port 3	Input/output	Programmable input/output port.
	P41–P47	Input/output port 4	Input/output	Programmable input/output port.
	P61–P63	Input/output port 6	Input/output	Programmable input/output port.
	P70–P77	Input/output port 7	Input/output	Programmable input/output port.
	P82–P87	Input/output port 8	Input/output	Programmable input/output port.
	P93–P97	Input/output port 9	Input/output	Programmable input/output port.
	P100–P107	Input/output port 10	Input/output	Programmable input/output port.
	P110–P117	Input/output port 11	Input/output	Programmable input/output port.
	P124–P127	Input/output port 12	Input/output	Programmable input/output port.
	P130–P137	Input/output port 13	Input/output	Programmable input/output port.
	P150, P153	Input/output port 15	Input/output	Programmable input/output port.
	P174, P175	Input/output port 17	Input/output	Programmable input/output port.
	P220, P221 P224, P225	Input/output port 22	Input/output	Programmable input/output port. (However, P221 is an input-only port)

Note 1: Input/output port 5 is reserved for future use. Input/output ports 14,16,18, 20 and 21 do not exist.

Outline of the CPU core

The 32182 Group is built around the M32R RISC CPU core, and has the instruction set common to all of the M32R family microcomputers. To achieve high-precision arithmetic operation, this microcomputer additionally incorporates a fully IEEE754 compliant, single-precision FPU.

Instructions are processed in five pipelined stages consisting of instruction fetch, decode, execution, memory access, and write back. Thanks to its "out-of-order-completion" mechanism, the M32R CPU allows clock cycle to realize efficient instruction execution control.

The M32R-FPU internally contains sixteen 32-bit general-purpose registers. The instruction set consists of 100 discrete instructions, which come in either 16-bit or 32-bit instruction format. Use of the 16-bit instruction format helps to reduce the program code size. Also, the availability of 32-bit instructions facilitates programming and increases the performance at the same clock speed, as compared to architectures with segmented address spaces.

Multiply-Accumulate instructions comparable to DSP

The M32R-FPU contains a multiplier/accumulator that can execute 32-bit × 16-bit in one cycle. Therefore, it executes a 32-bit × 32-bit integer multiplication instruction in three cycles.

Also, the M32R-FPU supports the following four multiply-Accumulate instructions (or multiplication instructions) for DSP function use.

(1) 16 high-order register bits × 16 high-order register bits
(2) 16 low-order register bits × 16 low-order register bits
(3) All 32 register bits × 16 high-order register bits
(4) All 32 register bits × 16 low-order register bits

Furthermore, the M32R-FPU has instructions for rounding the value stored in the accumulator to 16 or 32-bit, and instructions for shifting the accumulator value to adjust digits before storing in a register. Because these instructions also can be executed in one cycle, DSP comparable data processing capability can be obtained by using them in combination with high-speed data transfer instructions such as Load & Address Update or Store & Address Update.

FPU instructions (12 instructions)

The M32R-FPU supports single-precision, floating-point arithmetic operations fully compliant with IEEE754 standard. More specifically, it supports all of the following five exceptions and four rounding modes. Because the general-purpose registers are used for floating-point arithmetic, data transfer overhead is reduced.

- Five exceptions (invalid operation, division by zero, overflow, underflow, and inexact)
- Four rounding modes (round toward nearest, round toward zero, round toward +∞, round toward -∞)

Also included are the floating-point multiply and add (FMADD) and floating-point multiply and subtract (FMSUB) instructions suitable for butterfly operation in FFT.

Extended instructions (5 instructions)

The M32R-FPU has several instructions implemented in it as extended instructions such as those to set, clear, and test bits, those to set and clear data in the processor status register, and those to automatically increment the address in which to store a halfword.

Address space

The 32182 Group's logical address is always handled in width of 32-bit, providing a linear address space of up to 4G bytes. The 32182's address space is divided into the following spaces.

User space

A 2G-byte area from H'0000 0000 to H'7FFF FFFF is the user space. Located in this space are the user ROM area, external extended area, internal RAM area, and SFR (Special Function Register) area (internal peripheral I/O registers). Of these, the user ROM area and external extended area are located differently depending on mode settings.

System space

A 2G-byte area from H'8000 0000 to H'FFFF FFFF is the system area. This space is reserved for use by development tools such as an in-circuit emulator and debug monitor, and cannot be used by the user.

Built-in flash memory and RAM

The M32182F8VFP/M32182F8TFP contains 1024K bytes flash memory and 64K bytes RAM, the M32182F3VFP/M32182F3TFP contains 384K bytes flash memory and 64K bytes RAM.

The internal flash memory can be programmed while being mounted on the printed circuit board (on-board programming). Use of flash memory allows the same chip as those used in mass production to be used beginning with the development stage. This means that system development can be proceeded without having to change the printed circuit boards during the entire course, from prototype to mass production.

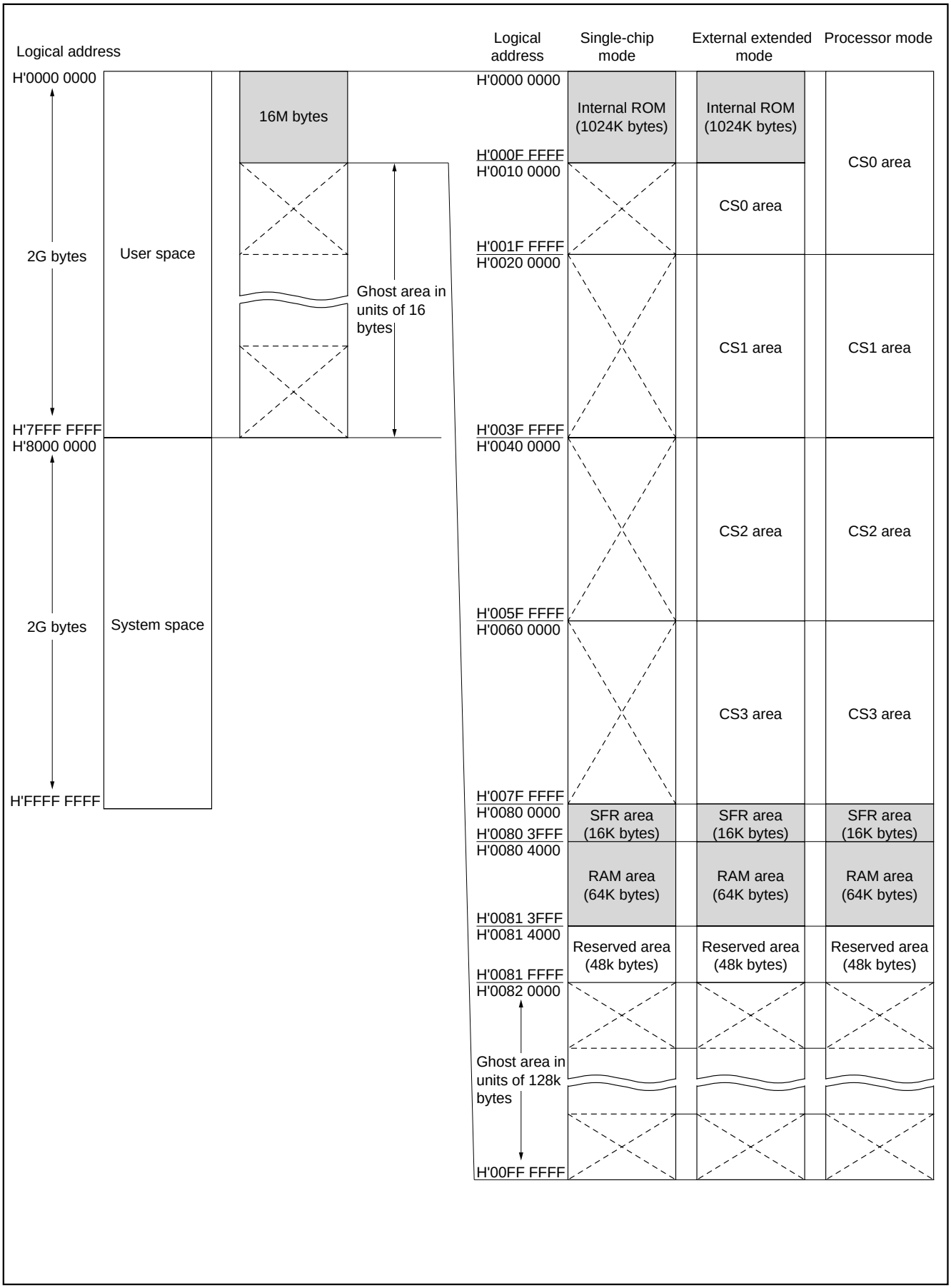


Figure 4. Address space of the M32182F8VFP/M32182F8TFP

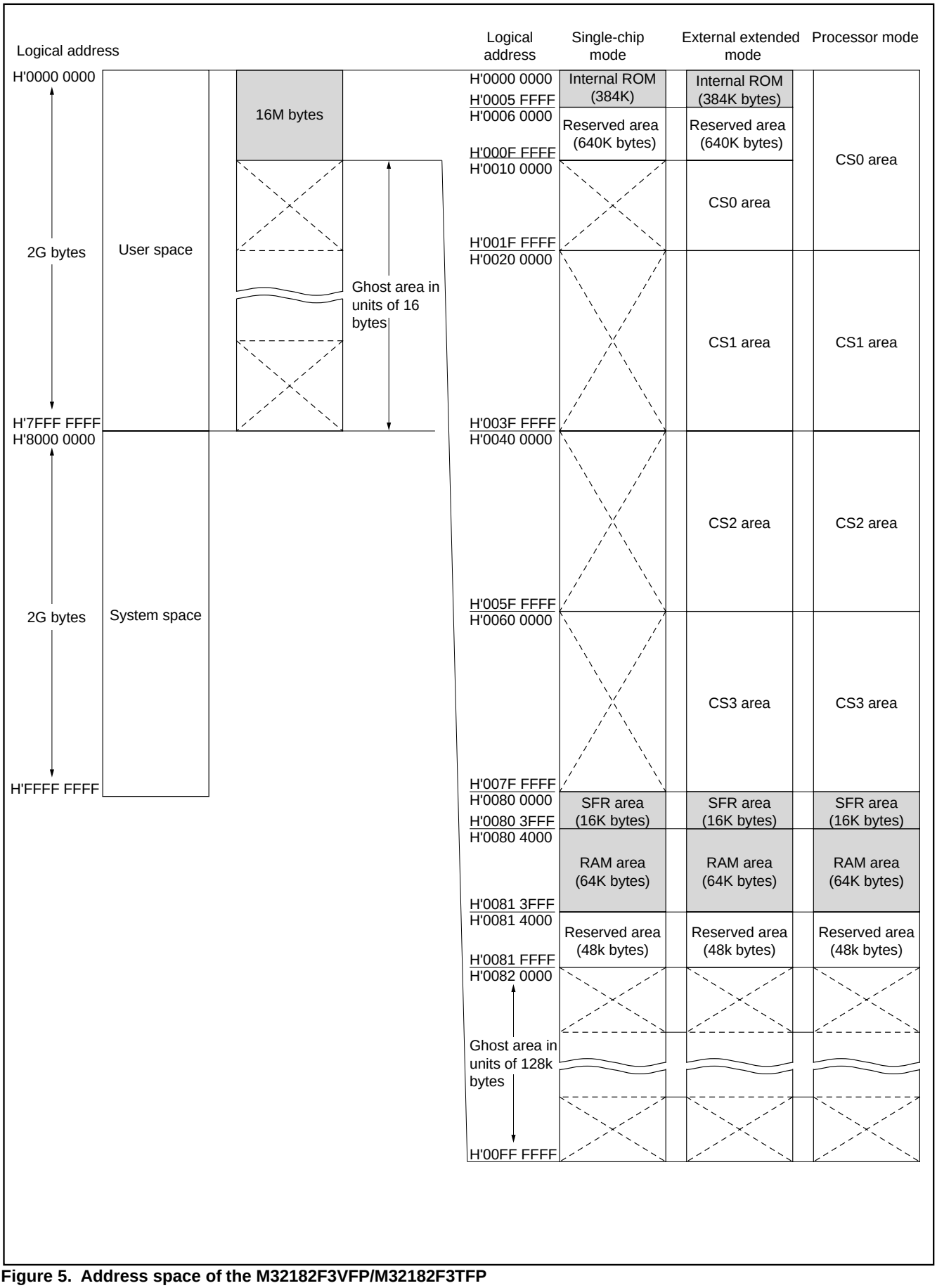


Figure 5. Address space of the M32182F3VFP/M32182F3TFP

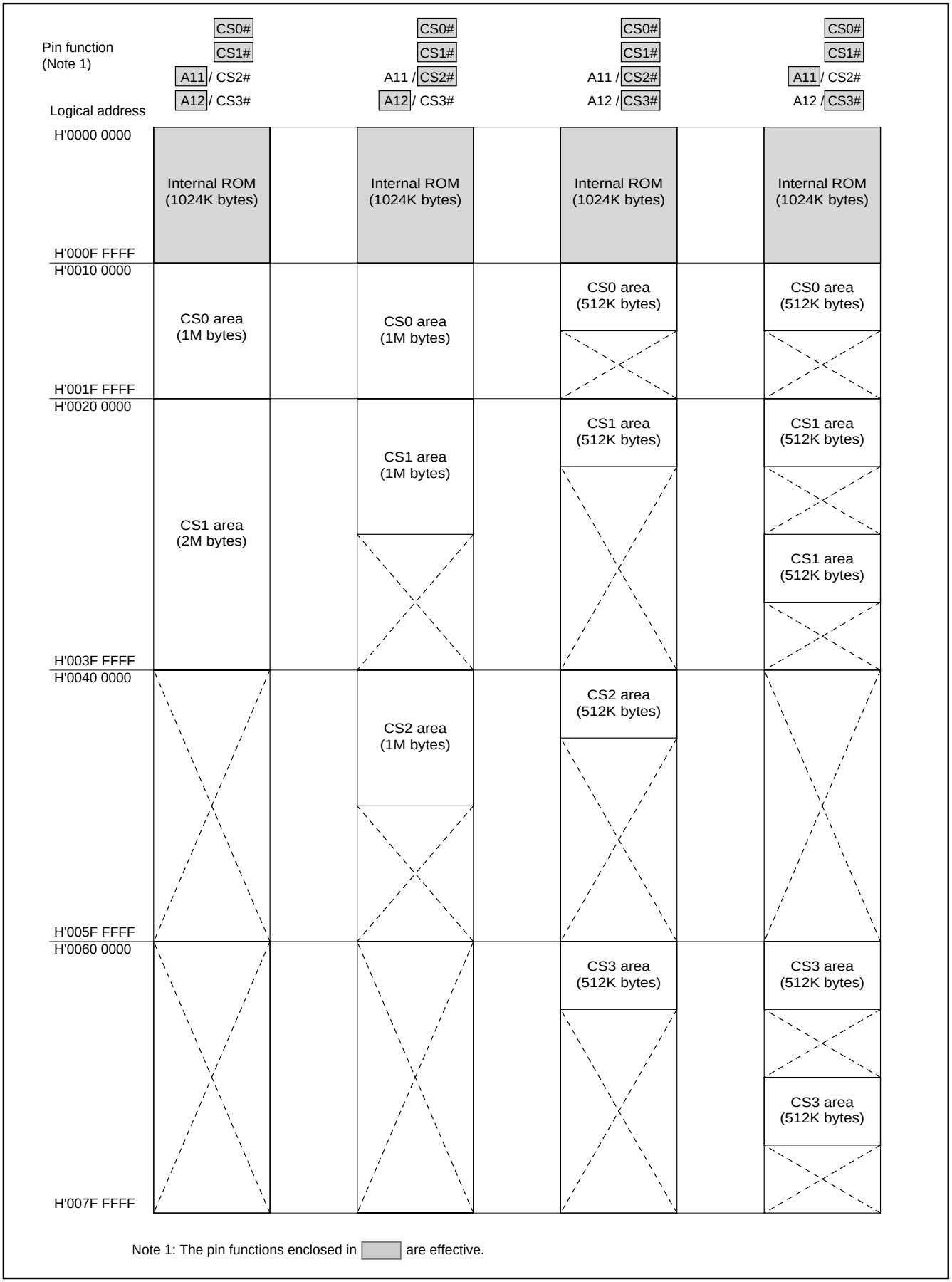


Figure 6. Internal ROM and External Extended Area when External Extended Mode (M32182F8VFP/M32182F8TFP)

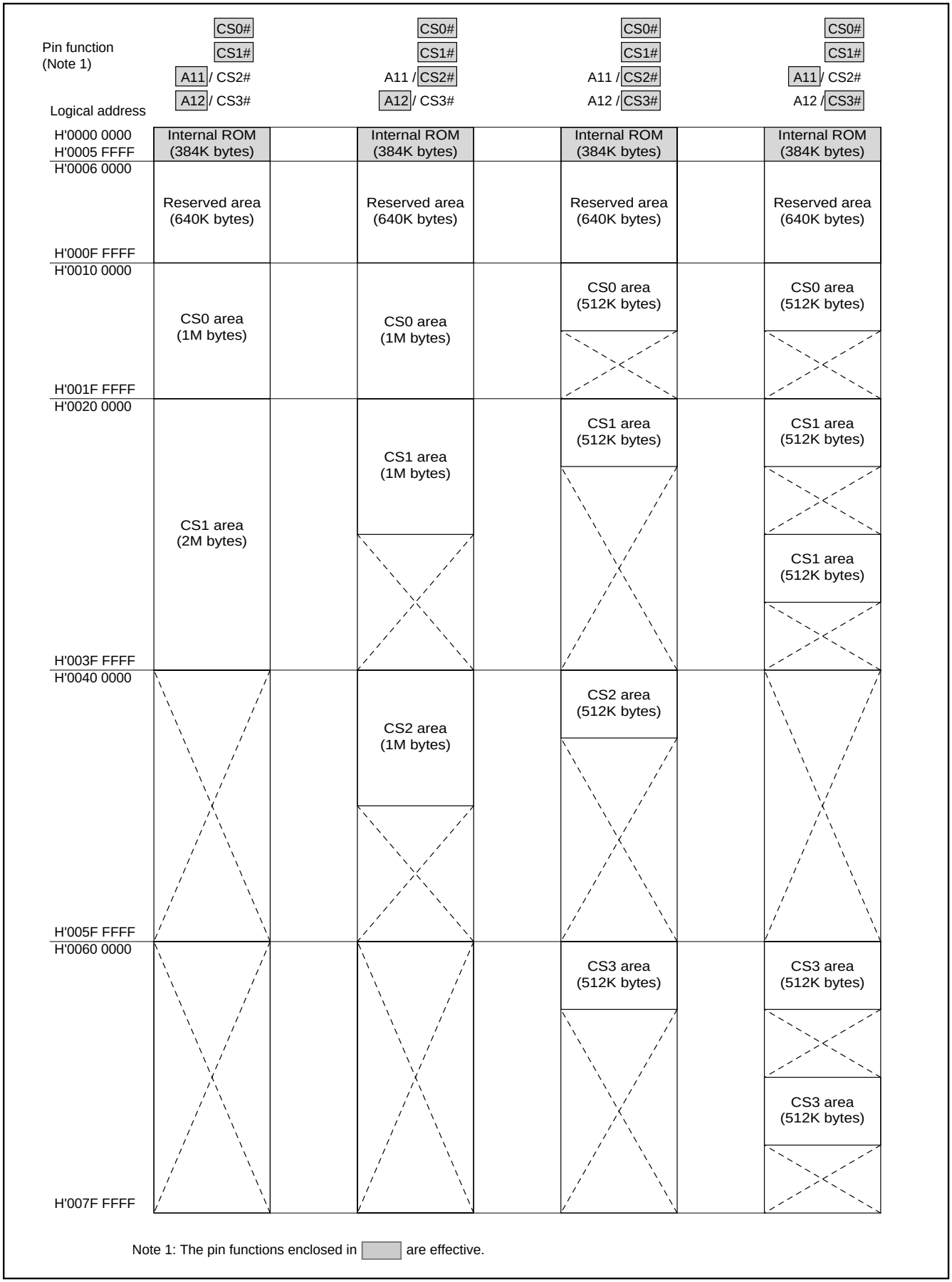


Figure 7. Internal ROM and External Extended Area when External Extended Mode (M32182F3VFP/M32182F3TFP)

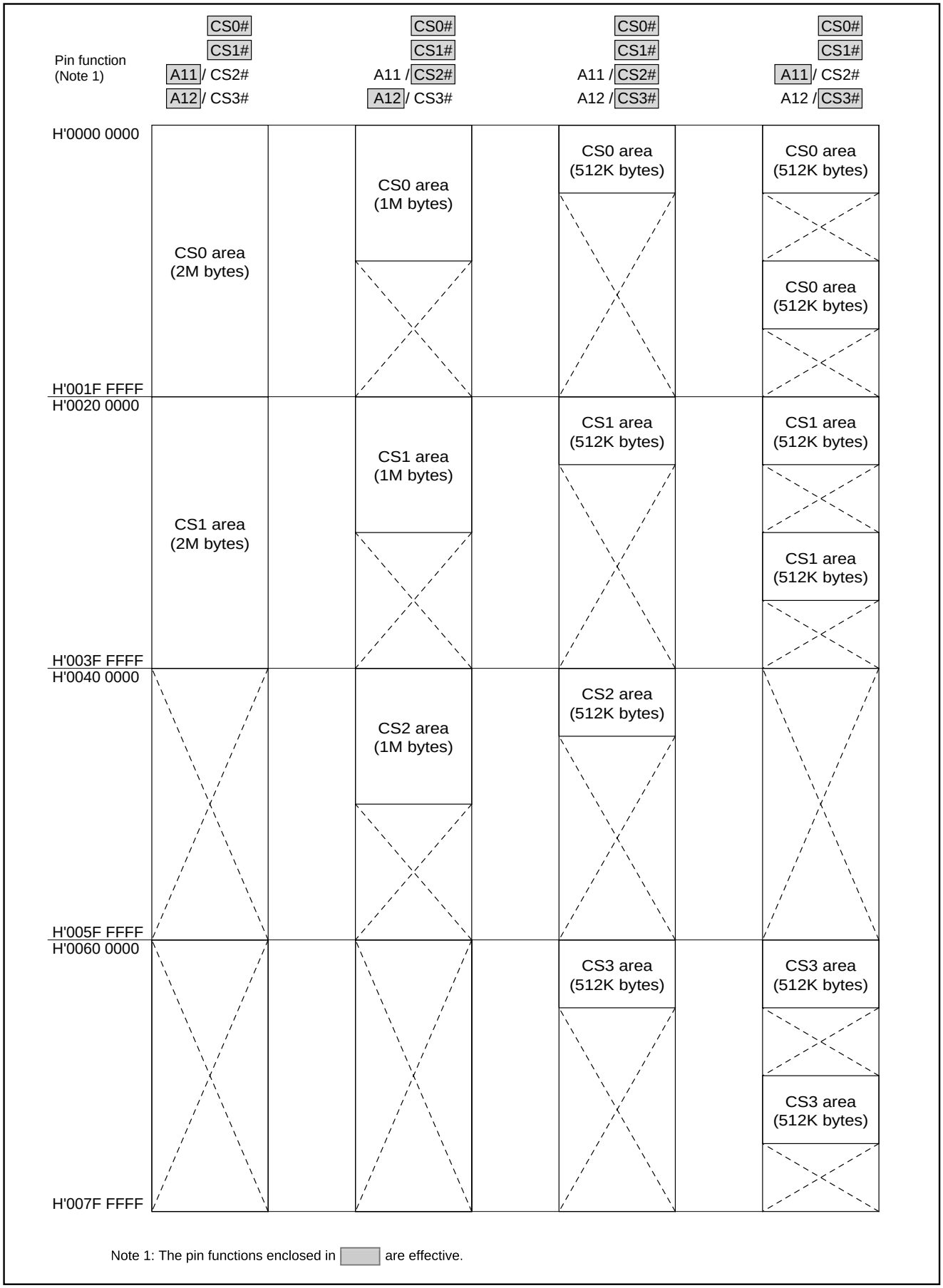
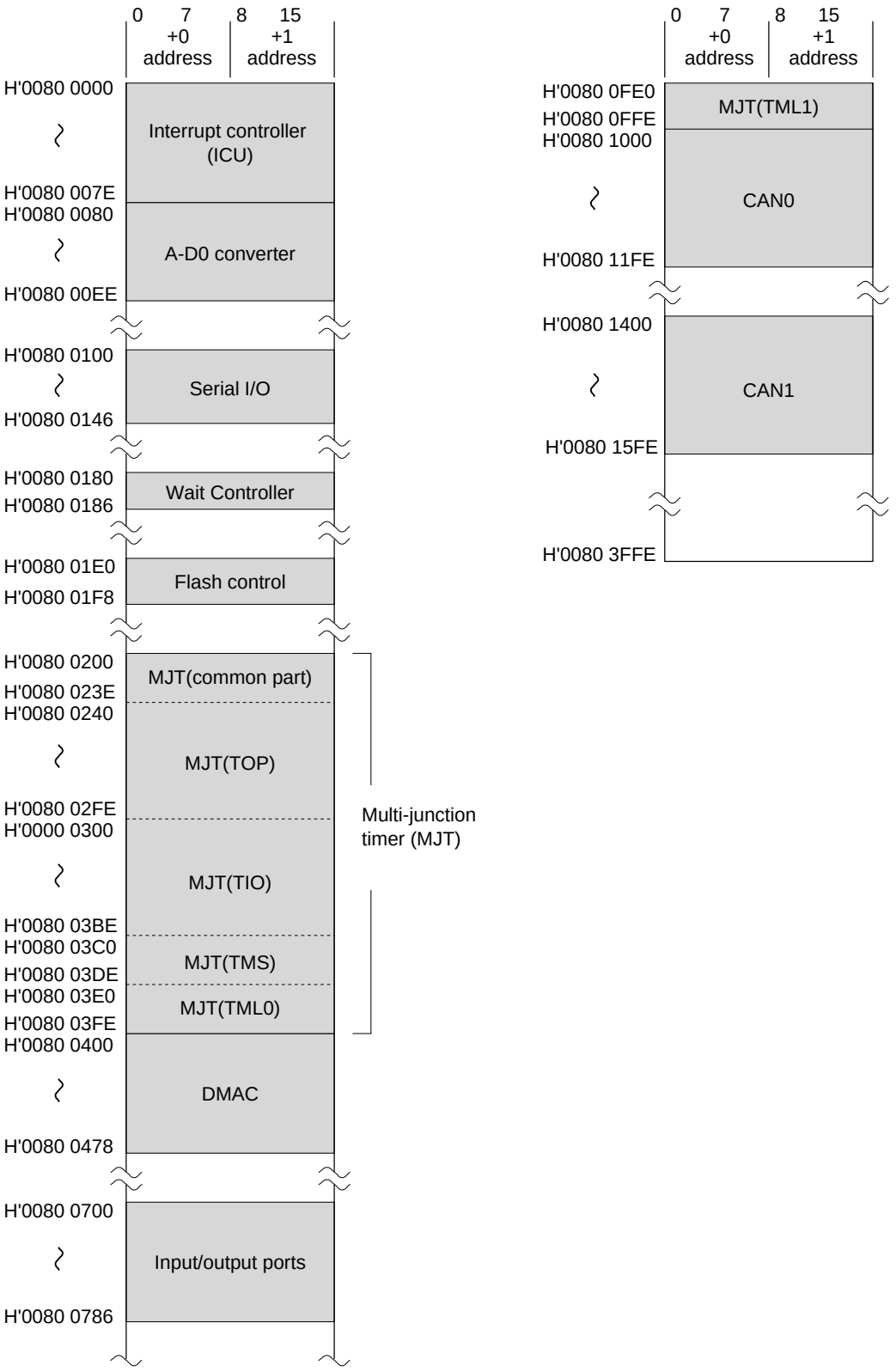


Figure 8. External Extended Area when Processor Mode



Note: • The Real-time debugger (RTD) is an independent module operated from external circuits, and is transparent to the CPU.

Figure 9. SFR Area

Built-in 37-channel multijunction timers (MJT)

The microcomputer contains a total of 37 channels of multijunction timers consisting of 11 channels of 16-bit output related timers, 10 channels of 16-bit input/output related timers, 8 channels of 16-bit input related timers, 8 channels of 32-bit input related timers. Each timer has multiple operation modes to choose from, depending on the purposes of use.

Also, the multijunction timers internally have a clock bus, input event bus, and an output event bus, so that multiple timers can be used in combination allowing for a flexible timer configuration. The output related timers have a correcting function that allows the timer's count value to be incremented or decremented as necessary while count is in progress, making real-time output control possible.

Table 4. Outline of the MJT

Name	Type	Number of channels	Contents
TOP (Timer Output)	Output related 16-bit timer (down-counter)	11	One of three output modes is selected in software. <With correcting function> • Single-shot output mode • Delayed single-shot output mode <Without correcting function> • Continuous output mode
TIO (Timer Input Output)	Input/output related 16-bit timer (down-counter)	10	One of three input modes and four output modes is selected in software. <Input mode> • Measure clear input mode • Measure free-run input mode • Noise processing input mode <Output mode without correcting function> • PWM output mode • Single-shot output mode • Delayed single-shot output mode • Continuous output mode
TMS (Timer Measure Small)	Input related 16-bit timer (up-counter)	8	16-bit input measure timer.
TML (Timer Measure Large)	32-bit timer (up-counter)	8	32-bit input measure timer.

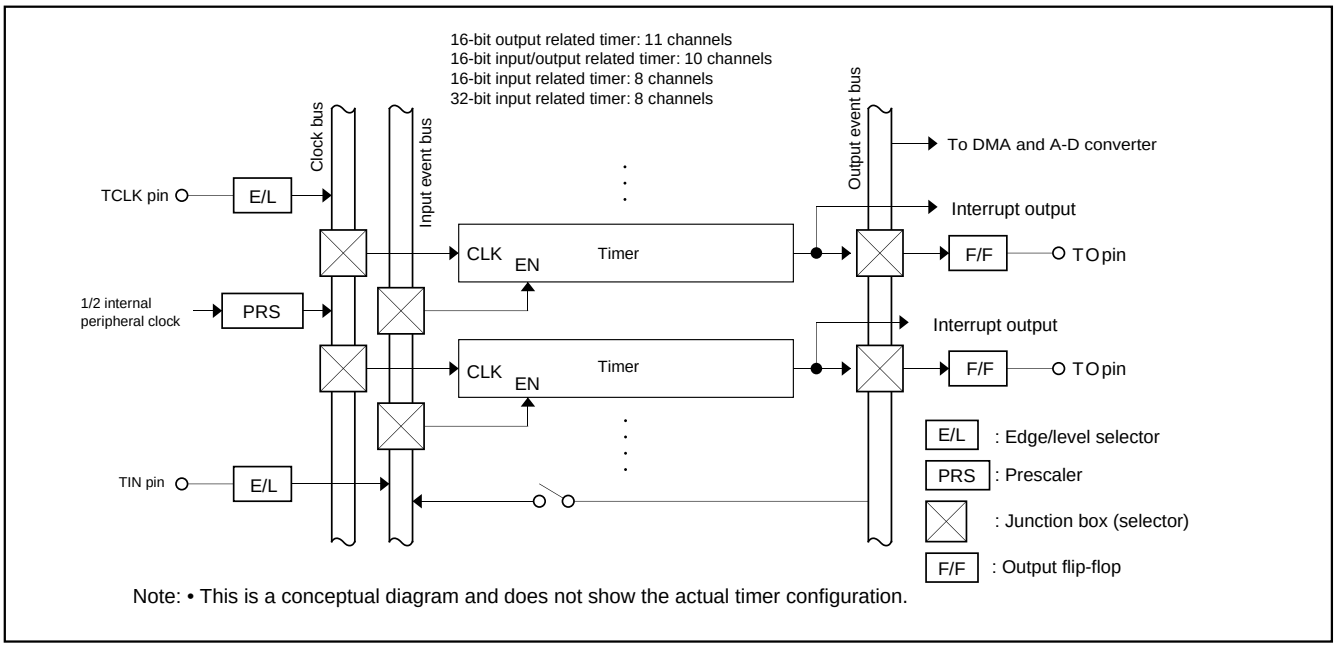
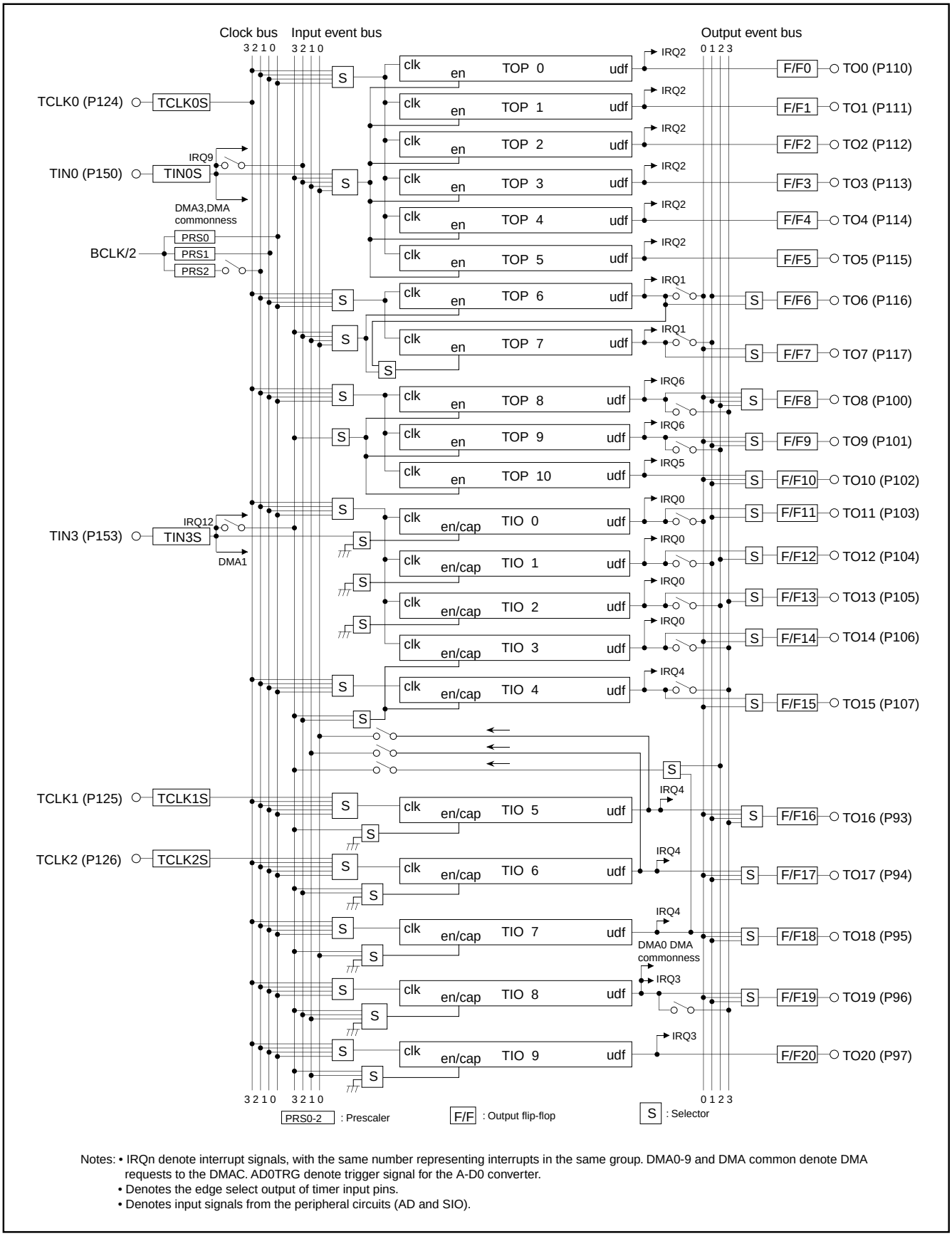


Figure 10. Conceptual Diagram of the Multijunction Timers (MJT)



Notes: • IRQn denote interrupt signals, with the same number representing interrupts in the same group. DMA0-9 and DMA common denote DMA requests to the DMAC. AD0TRG denote trigger signal for the A-D0 converter.
• Denotes the edge select output of timer input pins.
• Denotes input signals from the peripheral circuits (AD and SIO).

Figure 11. Block Diagram of MJT (1/3)

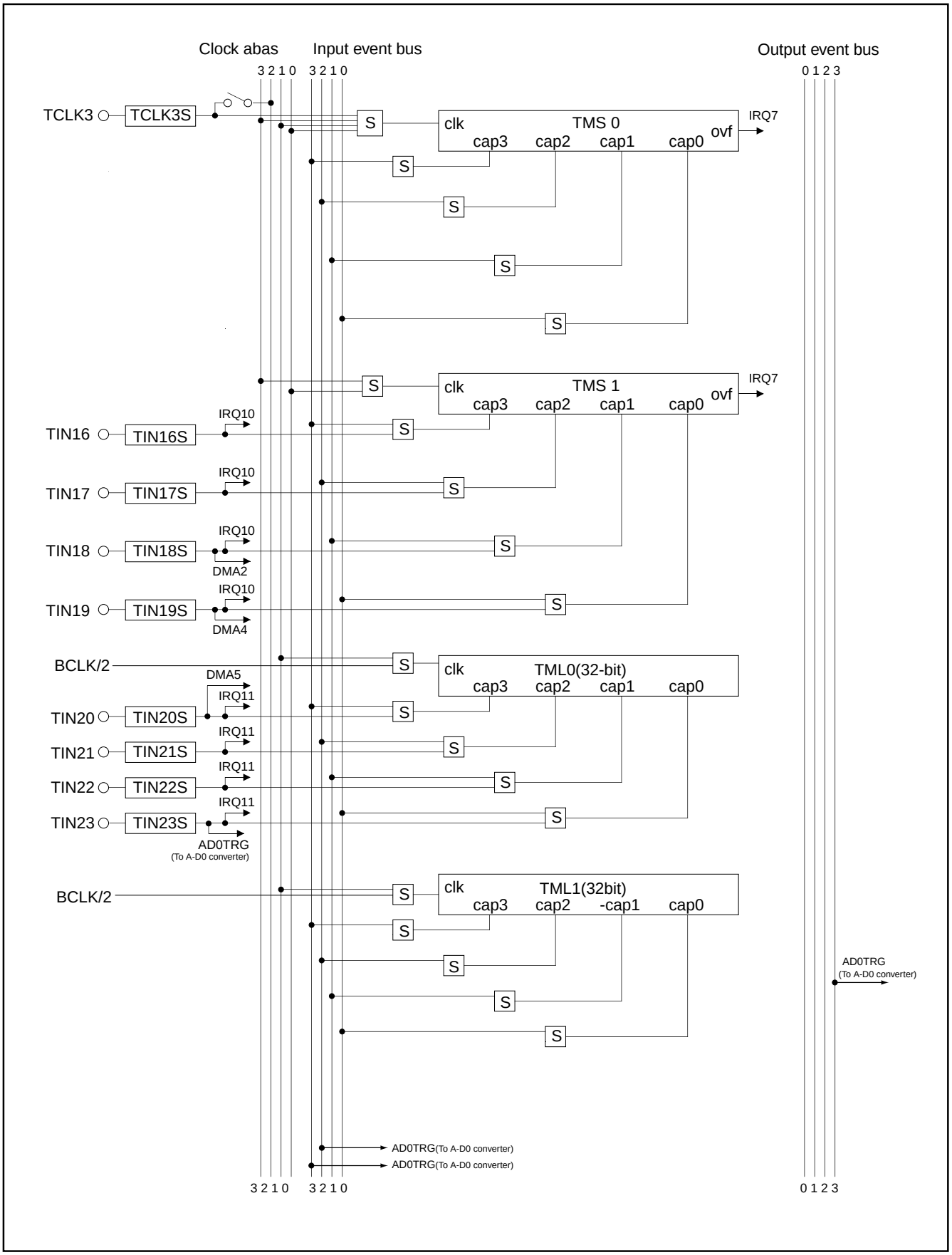


Figure 12. Block Diagram of MJT (2/3)

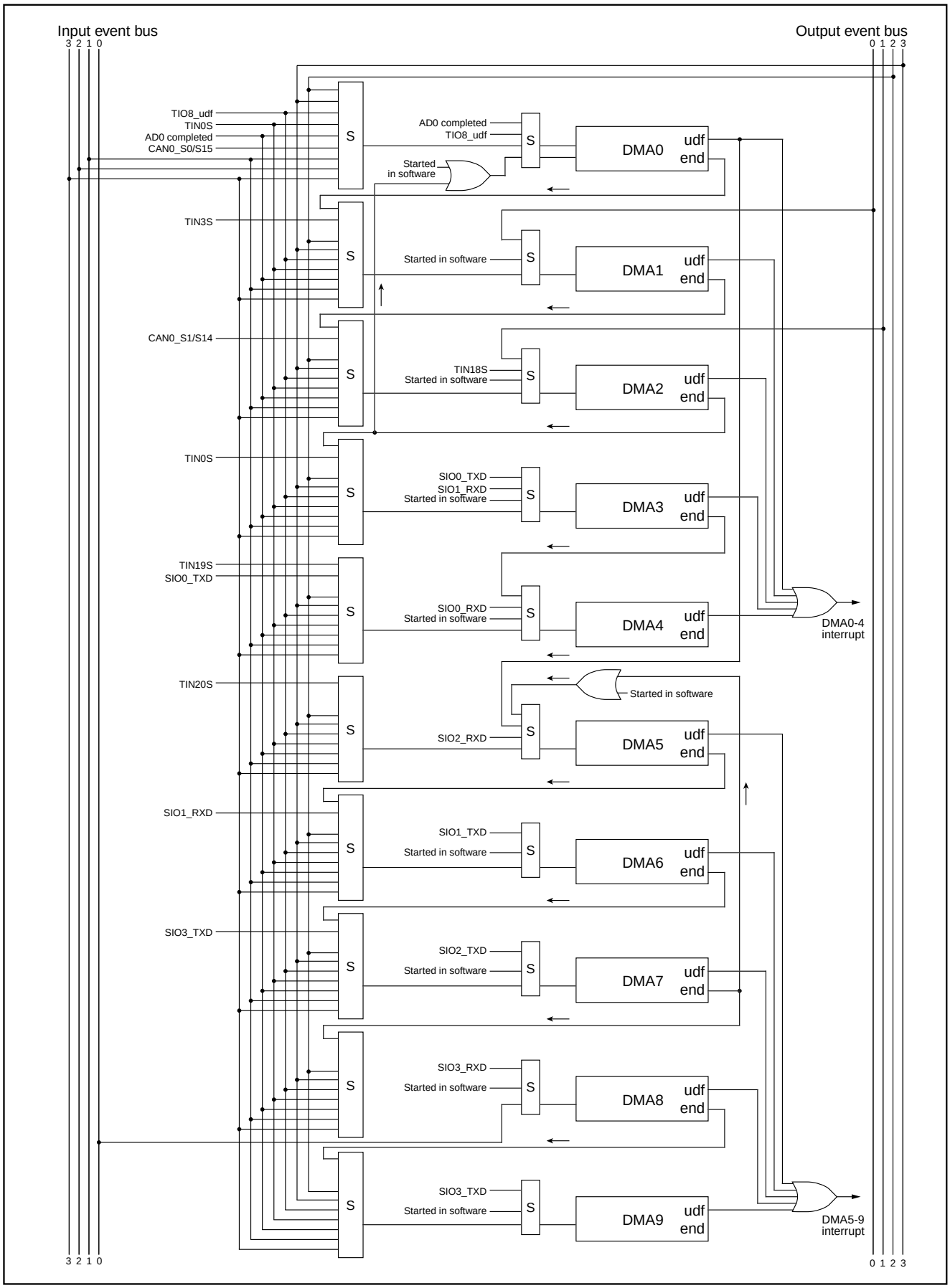


Figure 13. Block Diagram of MJT (3/3)

Built-in 10-Channel DMAC

The microcomputer contains 10 channels of DMAC, allowing for data transfer between internal peripheral I/Os, between internal RAM and internal peripheral I/O, and between internal RAMs.

DMA transfer requests can be issued from the user-created software, as well as can be triggered by a signal generated by the internal peripheral I/O (A-D converter, timer, or serial I/O).

The microcomputer also supports cascaded connection between DMA channels (starting DMA transfer on a channel at end of transfer on another channel). This makes advanced transfer processing possible without causing any additional CPU load.

Table 5. Outline of the DMAC

Item	Content
Number of channels	10 channels
Transfer request	• Software trigger • Request from internal peripheral I/O: A-D converter, timer, or serial I/O (reception completed, transmit buffer empty) • Cascaded connection between DMA channels possible (Note 1)
Maximum number of times transferred	65536 times
Transferable address space	• 64K bytes (address space from H'0080 0000 to H'0080 FFFF) • Transfers between internal peripheral I/Os, between internal RAM and internal peripheral IO, and between internal RAMs are supported
Transfer data size	16-bit or 8-bit
Transfer method	Single transfer DMA (control of the internal bus is relinquished for each transfer performed), dual-address transfer
Transfer mode	Single transfer mode
Direction of transfer	One of three modes can be selected for the source and destination of transfer: • Address fixed • Address increment • 32-channel ring buffer
Channel priority	Channel 0 > channel 1 > channel 2 > channel 3 > channel 4 > channel 5 > channel 6 > channel 7 > channel 8 > channel 9 (Fixed priority)
Maximum transfer rate	13.3M bytes per second (when internal peripheral clock = 20 MHz)
Interrupt request	Group interrupt request can be generated when each transfer count register underflows

Note 1: The following DMA channels can be cascaded.
DMA transfer on channel 1 started at end of one DMA transfer on channel 0
DMA transfer on channel 5 started at completion of all DMA transfers on channel 0 (transfer count register underflow)
DMA transfer on channel 2 started at end of one DMA transfer on channel 1
DMA transfer on channel 0 started at end of one DMA transfer on channel 2
DMA transfer on channel 3 started at end of one DMA transfer on channel 2
DMA transfer on channel 4 started at end of one DMA transfer on channel 3
DMA transfer on channel 6 started at end of one DMA transfer on channel 5
DMA transfer on channel 7 started at end of one DMA transfer on channel 6
DMA transfer on channel 5 started at end of one DMA transfer on channel 7
DMA transfer on channel 8 started at end of one DMA transfer on channel 7
DMA transfer on channel 9 started at end of one DMA transfer on channel 8

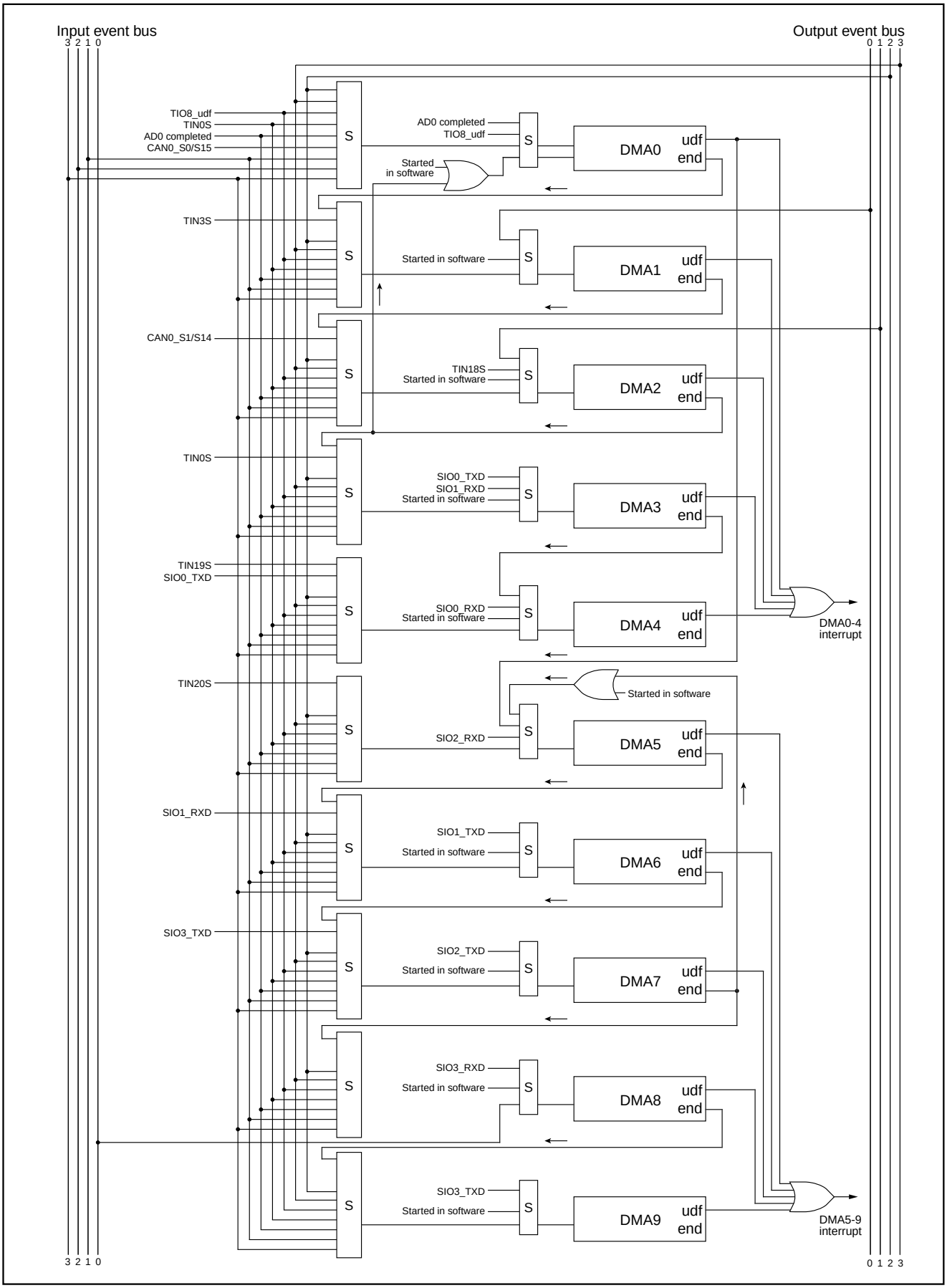


Figure 14. Block Diagram of DMAC

12-channel A-D Converters

The microcomputer contains 12-channel A-D converters with 10-bit resolution. In addition to single conversion on each channel, continuous A-D conversion on a combined group of N (N = 1–12) channels is possible. The A-D converted value can be read out in either 10-bit or 8-bit.

In addition to ordinary A-D conversion, the converters support comparator mode in which the set value and A-D converted value are compared to determine which is larger or smaller than the other.

Moreover, there is also Sample & hold function, input voltage is sampled, when A-D conversion is started, and the A-D conversion of the sampling voltage is carried out.

Since there is no invalid domain near [which becomes a problem by the external operational amplifier etc.] VCCE/VSS, conversion by the full range is possible in this sample & hold circuit.

When A-D conversion is finished, the converters can generate a DMA transfer request, as well as an interrupt.

The A-D converters are interfaced using a dedicated power supply to allow for connections to the peripheral circuits operating with 5 V.

Table 6. Outline of the A-D Converters

Item	Content				
Analog input	12-channel				
A-D conversion method	Successive approximation method				
Resolution	10-bit (Conversion results can be read out in either 10 or 8-bit)				
Absolute accuracy (conditions: Ta = 25°C, AVCC0, 1 = VREF0, 1 = 5.12 V)	During low speed mode: Normal mode: ± 2 LSB, double speed mode: ± 2 LSB (Note 1)				
	During high speed mode: Normal mode: ± 3 LSB, double speed mode: ± 3 LSB (Note 1)				
Conversion mode	A-D conversion mode, comparator mode				
Operation mode	Single mode, scan mode				
Scan mode	Single-shot scan mode, continuous scan mode				
Special mode	Single mode forcible execution under scan mode operation, scan mode start after the single mode execution, conversion re-start				
Sample & hold function	Input voltage is sampled when A-D conversion is started, and it is A-D conversion about sampling voltage.				
Conversion start trigger	Software start	Started by setting A-D conversion start bit to 1			
	Hardware start	MJT input event bus 2, MJT input event bus 3, MJT output event bus 3, and TIN23			
Conversion Speed f(BCLK) : Internal peripheral clock operating frequency	During single mode (Unavailable for Sample & Hold Available for Normal Sample & Hold)	Low-speed mode	Normal	299	×1/f(BCLK) (Note 2)
			Double speed	173	×1/f(BCLK)
		High-speed mode	Normal	131	×1/f(BCLK)
			Double speed	89	×1/f(BCLK)
	During single mode (Available for High-speed Sample & Hold)	Low-speed mode	Normal	191	×1/f(BCLK)
			Double speed	101	×1/f(BCLK)
		High-speed mode	Normal	95	×1/f(BCLK)
			Double speed	53	×1/f(BCLK)
	During comparator mode	Low-speed mode	Normal	47	×1/f(BCLK)
			Double speed	29	×1/f(BCLK)
		High-speed mode	Normal	23	×1/f(BCLK)
			Double speed	17	×1/f(BCLK)
Interrupt request generation	When A-D conversion is finished, when comparate operation is finished				
	When single-shot scan is finished, or when one cycle of continuous scan is finished				
DMA transfer request generation	When A-D conversion is finished, when comparate operation is finished				
	When single-shot scan is finished, or when one cycle of continuous scan is finished				

Note 1: The performance is the same during sample & hold function.
Note 2: When XIN = 10 MHz, f(BLCK) = 20 MHz.

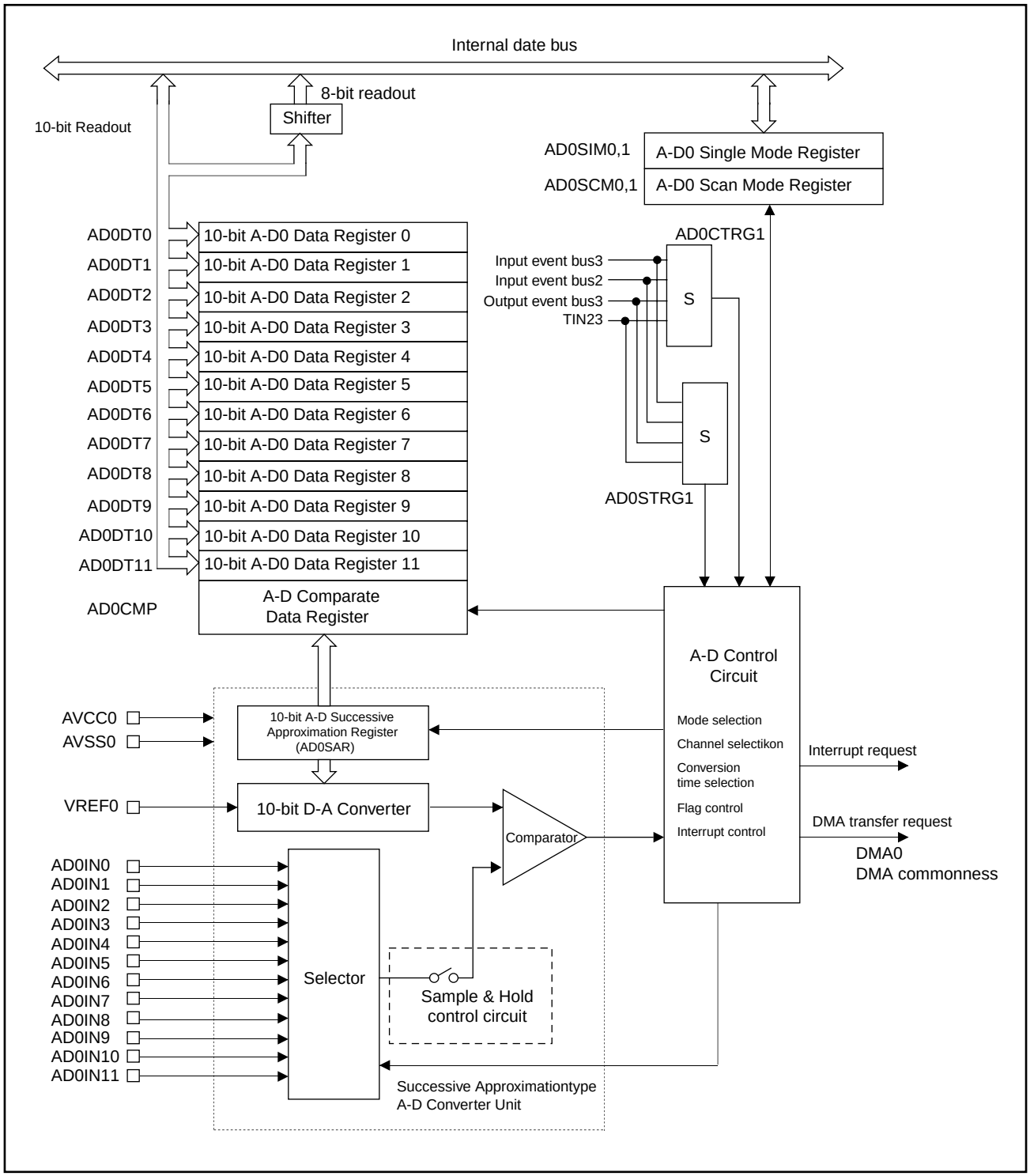


Figure 15. Block Diagram of the A-D0 Converter

4-channel High-speed Serial I/Os

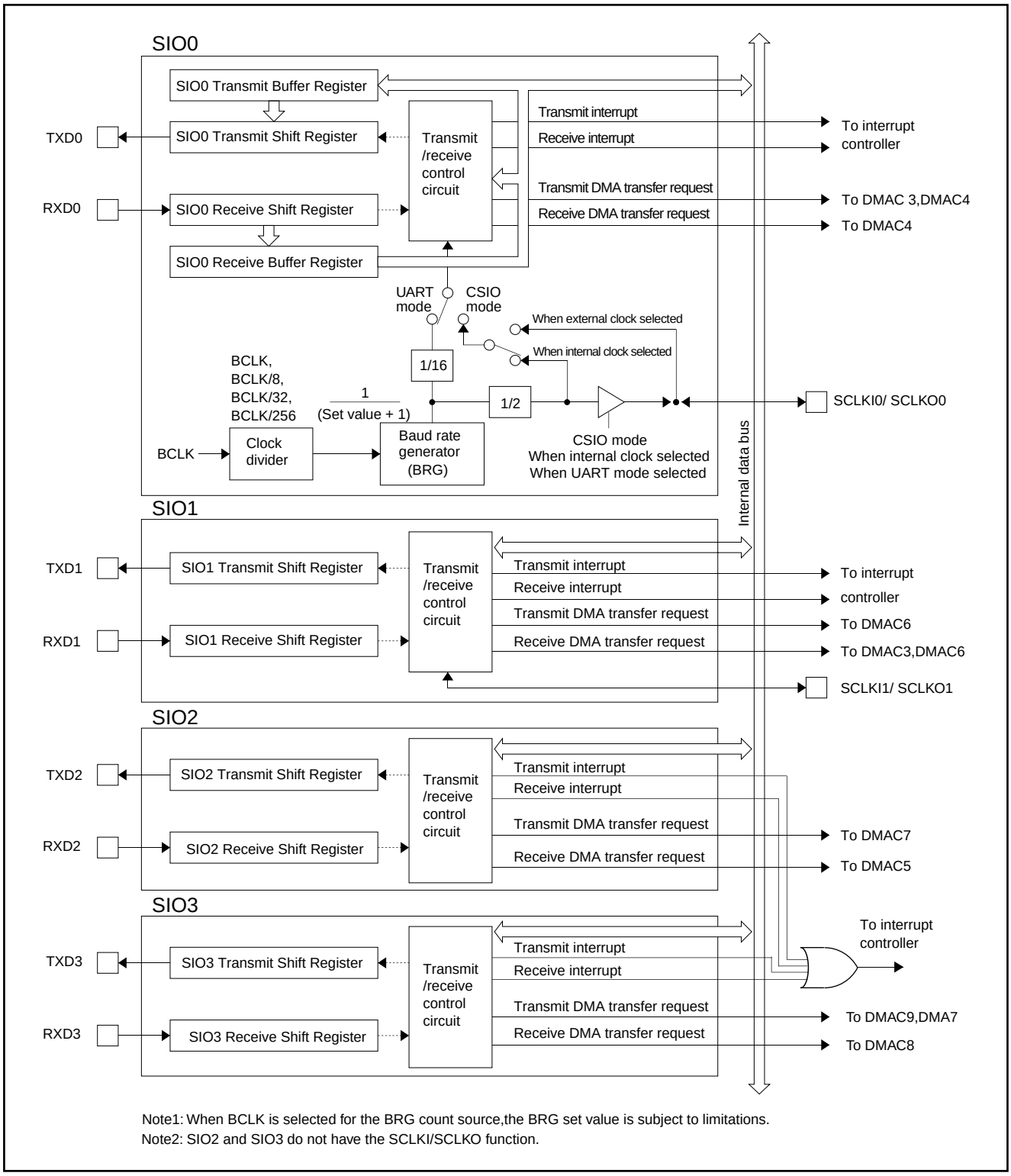
The microcomputer contains 4 channels of serial I/Os consisting of four channels that can be set for CSIO mode (clock-synchronized serial I/O) or UART mode (asynchronous serial I/O) and two other channels that can only be set for UART mode.

The SIO has the function to generate a DMA transfer request when data reception is completed or the transmit register becomes empty, and is capable of high-speed serial communication without causing any additional CPU load.

Table 7. Outline of the Serial I/O

Item	Content
Number of channels	CSIO/UART: 2 channels (SIO0, SIO1) UART only : 2 channels (SIO2, SIO3)
Clock	During CSIO mode : Internal clock / external clock, selectable (Note 1) During UART mode: Internal clock only
Transfer mode	Transmit half-duplex, receive half-duplex, transmit/receive full-duplex
BRG count source	f(BCLK), f(BCLK)/8, f(BCLK)/32, f(BCLK)/256 (When internal clock is selected) (Note 2)
Data format	CSIO mode: Data length = Fixed to 8-bit Order of transfer = Fixed to LSB first UART mode: Start bit = 1-bit Character length = 7, 8, or 9-bit Parity bit = With or without (If included, selectable between odd and even parity) Stop bit = 1 or 2-bit Order of transfer = Fixed to LSB first
Baud rate	CSIO mode: 152-bit per second to 2M-bit per second (when operating with f(BCLK) = 20 MHz) UART mode: 19-bit per second to 156K-bit per second (when operating with f(BCLK) = 20 MHz)
Error detection	CSIO mode: Overrun error only UART mode: Overrun, parity, and framing errors (The error-sum bit indicates which error has occurred)
Fixed cycle clock output function	When SIO0 or SIO1 is in UART mode, this function outputs a 1/2 BRG clock from the SCLK pin.

Note 1: During CSIO mode, the maximum input frequency of an external clock is f(BCLK) divided by 16.
Note 2: When f(BCLK) is selected for the BRG count source, the BRG set value is subject to limitations.



Note1: When BCLK is selected for the BRG count source,the BRG set value is subject to limitations.
Note2: SIO2 and SIO3 do not have the SCLKI/SCLKO function.

Figure 16. Block Diagram of Serial I/O

Input/output Ports

The microcomputer has a total of 97 input/output ports (of which P5 is reserved for future use). The input/output ports can be used as input ports or output ports by setting up their direction registers. Each input/output port is a dual-function pin shared with other internal peripheral I/O or external extended bus signal lines. These pin functions are selected by using the chip operation mode select or the input/output port operation mode registers.

Table 8. Outline of Input/output Ports

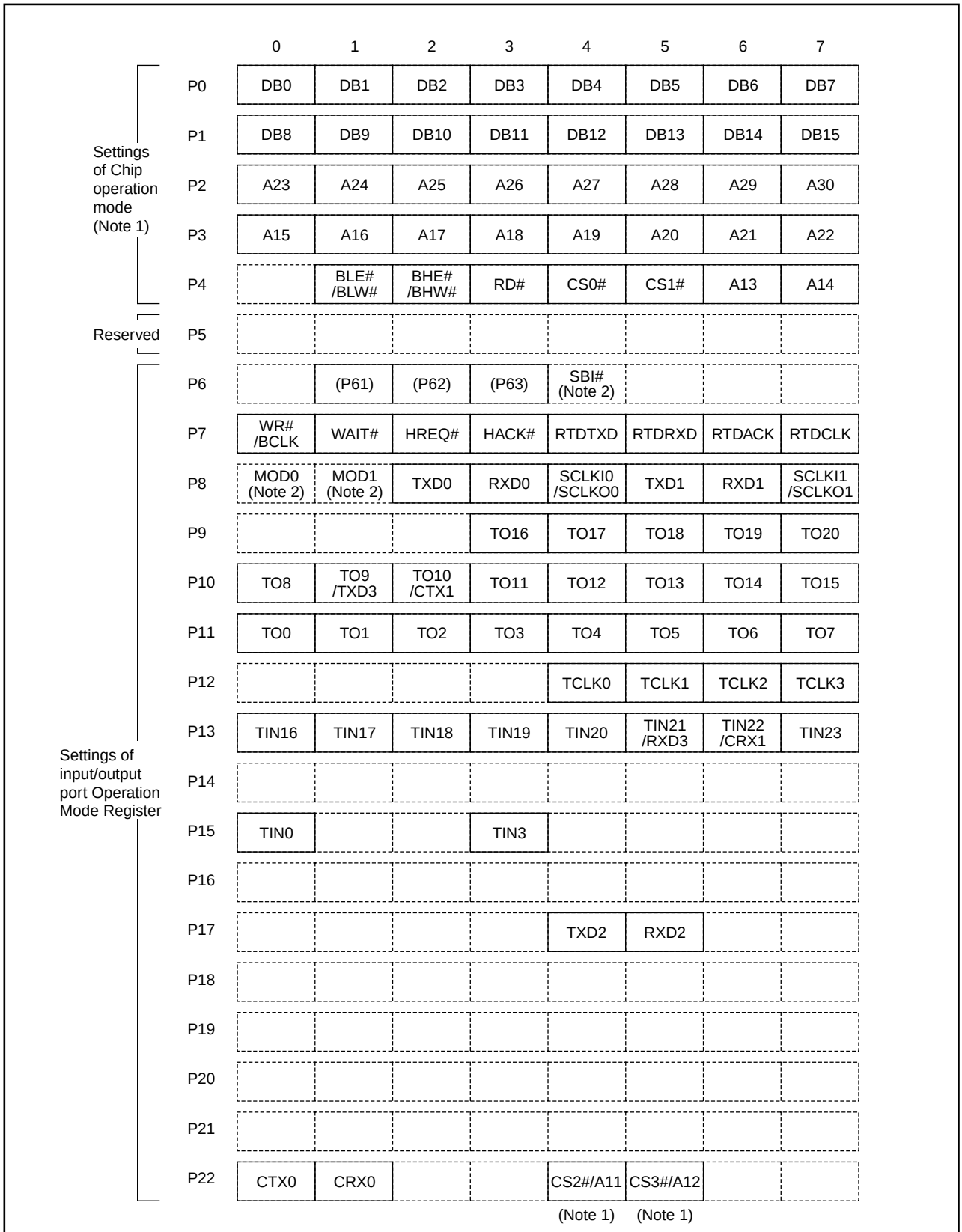
Item	Specification			
Number of Port	Total 97 ports			
	P0	:	P00–P07	(8 lines)
	P1	:	P10–P17	(8 lines)
	P2	:	P20–P27	(8 lines)
	P3	:	P30–P37	(8 lines)
	P4	:	P41–P47	(7 lines)
	P6	:	P61–P63	(3 lines)
	P7	:	P70–P77	(8 lines)
	P8	:	P82–P87	(6 lines)
	P9	:	P93–P97	(5 lines)
	P10	:	P100–P107	(8 lines)
	P11	:	P110–P117	(8 lines)
	P12	:	P124–P127	(4 lines)
	P13	:	P130–P137	(8 lines)
	P15	:	P150, P153	(2 lines)
	P17	:	P174, P175	(6 lines)
	P22	:	P220, P221, P224, P225	(4 lines)
Port function	The input/output ports can be set for input or output mode bit wise by using the input/output port direction control register. (However, P221 is CAN0 input-only port.)			
Pin function	Dual-functions shared with peripheral I/O or external extended signals (or multi-functions shared with peripheral I/Os which have multiple functions)			
Pin function change over	P0–4, P224–P227: Changed by setting CPU operation mode (MOD0 and MOD1 pins) (Note 1) P6-22 : Changed by setting the input/output port operation mode register (However, peripheral I/O pin functions are selected using the peripheral I/O register.)			

Note 1: When the CPU is operating in external extended mode, P0–P4 and P224, and P225 by default are set for input/output port pins, but have their functions switched for external extended signal pins by setting the Port Operation Mode Register. When operating in single-chip or processor mode, the pin functions are switched over by setting the CPU operation mode pins as shown in Table 8.

Table 8. CPU Operation Modes and P0–P4, P224, P225 Pin Functions

MOD0	MOD1	Operation mode	P0–P4, P224, P225 pin function
VSS	VSS	Single-chip mode	Input/output port pin
VSS	VCCE	External extended mode	Input/output port pin or External extended signal pin
VCCE	VSS	Processor mode (FP pin = VSS)	External extended signal pin
VCCE	VCCE	Do not select	-

Note: • VCCE and VSS are connected to power supply and GND, respectively.



Note: • P5, P14, P16, P18, P19, P20, and P21 do not exist.
Note 1: Pin functions are switched over by setting MOD0 and MOD1 pins.
Note 2: It cannot be used as a function of an input/output ports. The input level of SBI#, MOD0, and an MOD1 pin can be read.

Figure17. Input/Output Ports and pin function Assignments

CAN Modules

The 32182 contains two blocks of Full-CAN modules compliant with CAN Specification V2.0B active.

The CAN modules each have 16 slots of Message Slot.

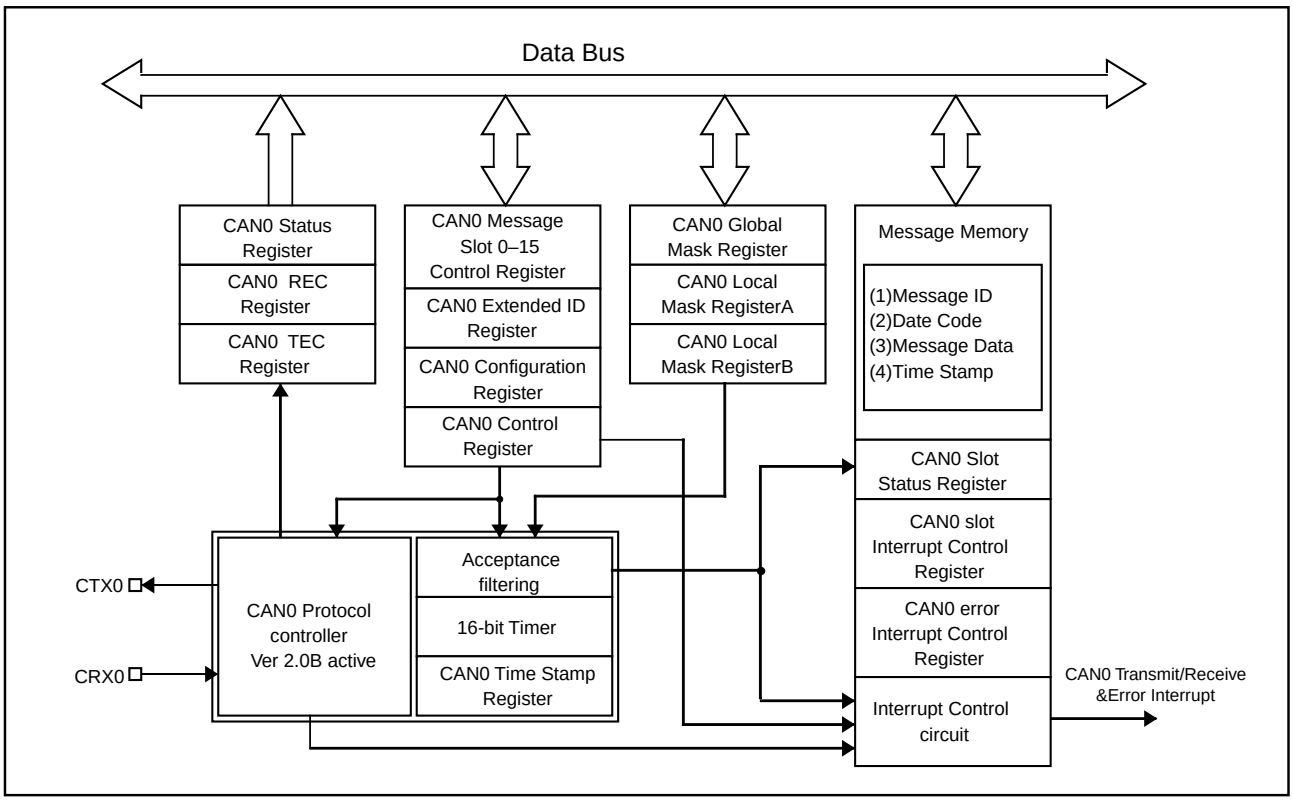


Figure 18. Block Diagram of the CAN0 Module

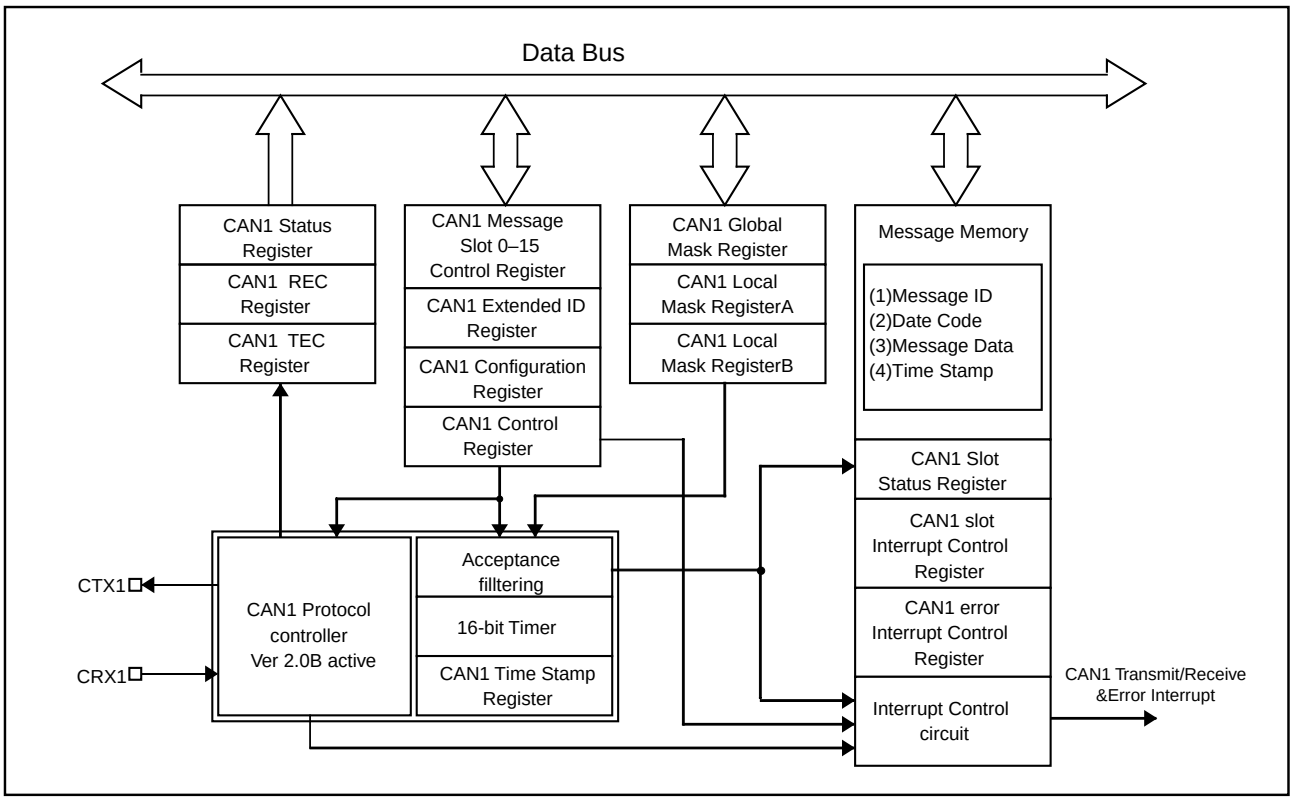


Figure 19. Block Diagram of the CAN1 Module

8-level Interrupt Controller

The Interrupt Controller controls interrupt requests from each internal peripheral I/O (23 sources) by using eight priority levels assigned to each interrupt source, including interrupts prohibition. In addition to these interrupts, it handles System Break Interrupt (SBI), Reserved Instruction Exception (RIE), and Address Exception (AE) as non-maskable interrupts.

Wait Controller

The Wait Controller supports access to external devices.
For access to an external extended area of up to 8M bytes (during external extended or processor mode), the Wait Controller controls bus cycle extension by inserting zero to seven wait cycles and using external WAIT# signal input.
However, as setup for lead of CS signal / lead of strobe signal / recovery / idol after lead cycle, only operation by "nothing" setup is guaranteed when 0wait is selected.
Moreover, WAIT by the external WAIT input is not received when 0wait is selected.

Built-in clock frequency multiplier

The PLL (clock frequency multiplier) multiplies the input clock frequency by 8 to generate the CPU memory clock. For the maximum CPU memory clock frequency of 80 MHz, the input clock frequency is 10.0 MHz.

Three operation modes

The 32182 Group has three operation modes: single-chip mode, external extended mode, and processor mode. These operation modes are changed from one to another by setting the MOD0 and MOD1 pins.

Port input threshold level select function

The port input level switch function sets the port threshold value to 3 different voltage levels (Schmidt ON/OFF selection also available).

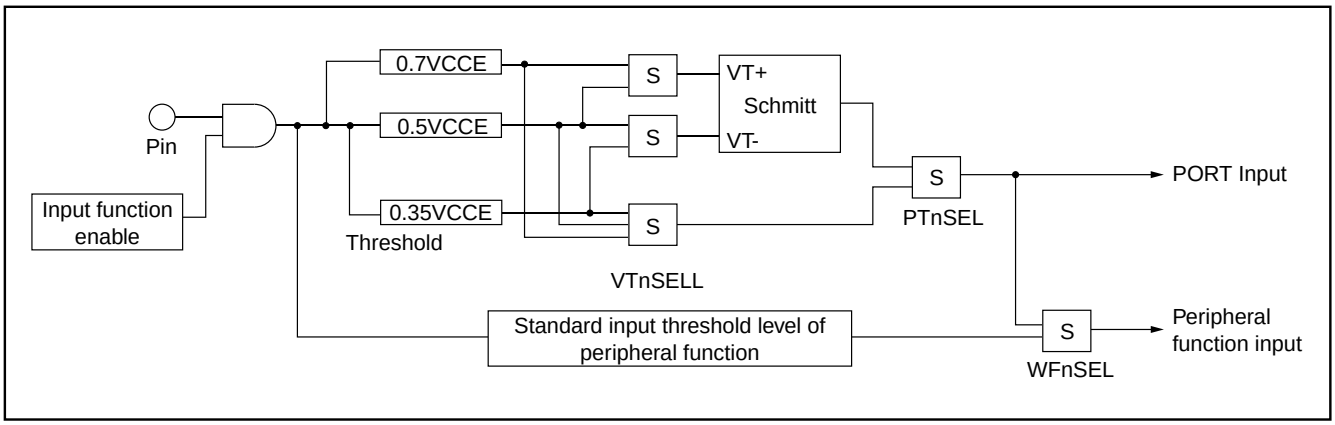


Figure 20. Port input threshold level select function

Real-time Debugger (RTD)

The Real-time Debugger (RTD) provides a function for accessing directly from the outside to the internal RAM. It uses a dedicated clock-synchronized serial I/O to communicate with the outside.

Use of the RTD communicating via dedicated serial lines allows the internal RAM to be read out and rewritten without having to halt the CPU. Also, it can activate an exclusive RTD interrupt through RTD communication.

Built-in Virtual-Flash emulation function

The 384K bytes of internal flash memory can have its 4K bytes areas (total 96 banks) replaced with 4K bytes areas of the internal RAM (4K bytes × 8). Use of this function helps to make the necessary changes and evaluate the changed program during development phase without having to reset the microcomputer. Also, when combined with the Real-time Debugger, this function enables the data in RAM to be rewritten and read out without causing CPU load, making it possible to reduce the program evaluation period.

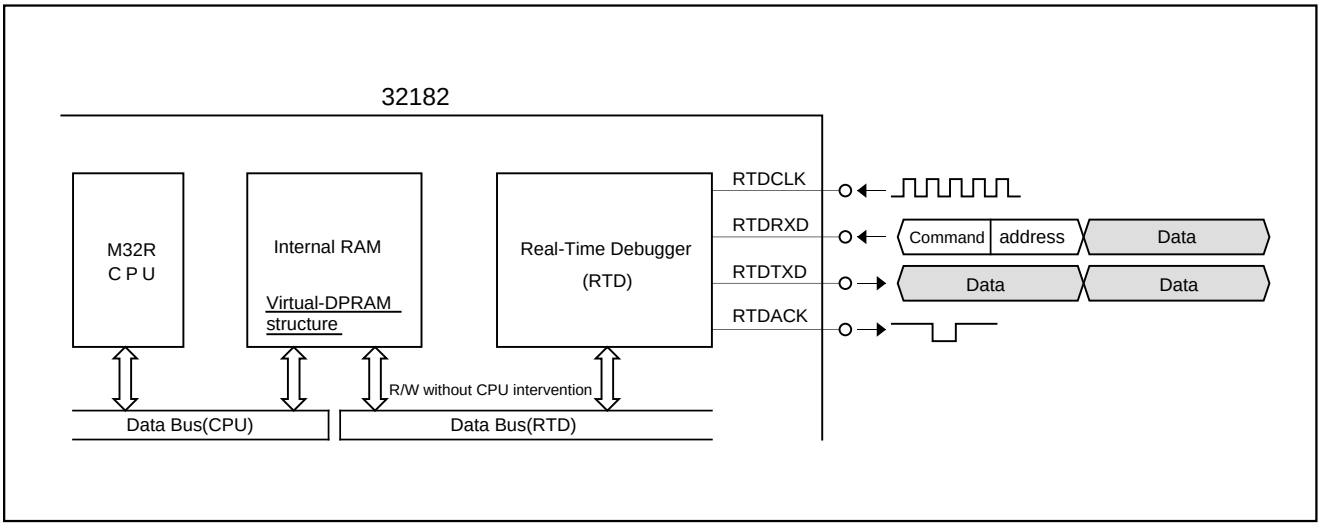
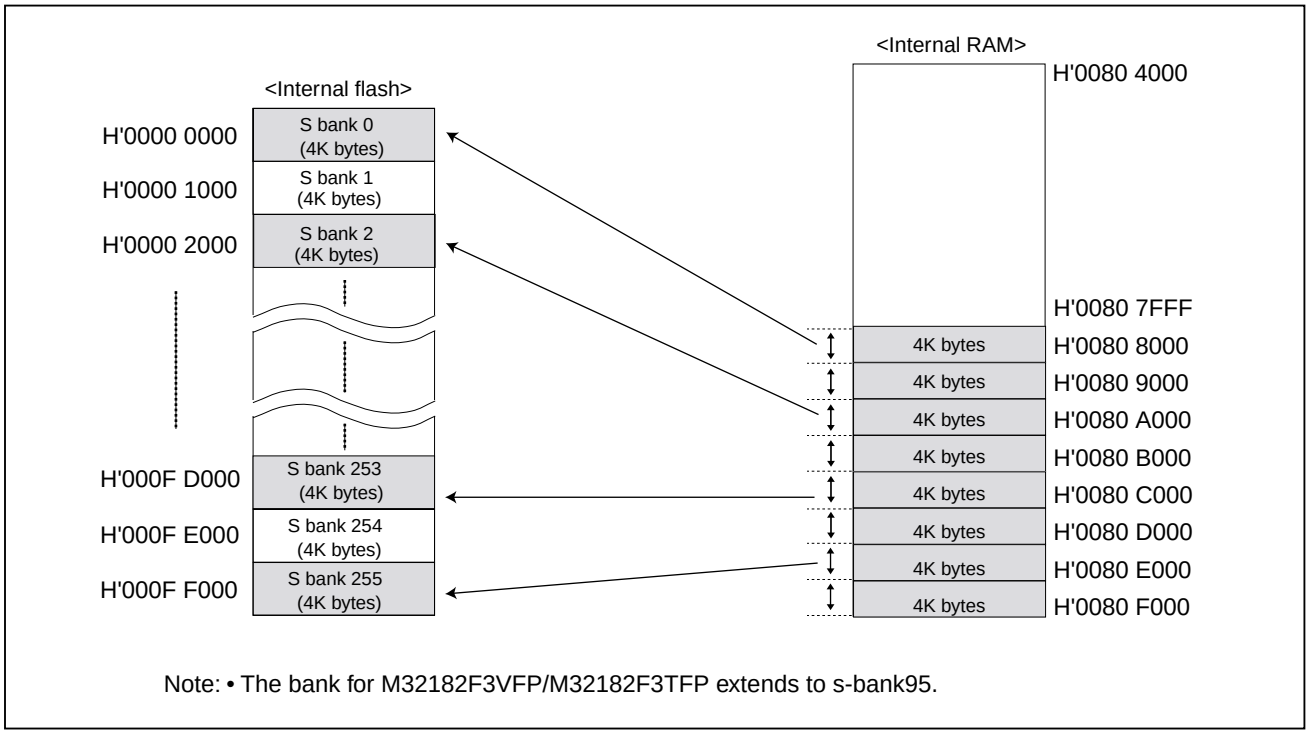


Figure 21. Conceptual Diagram of the Real-time Debugger (RTD)



Note: • The bank for M32182F3VFP/M32182F3TFP extends to s-bank95.

Figure 22. Conceptual Diagram of the Virtual -Flash Emulation (Units 4K bytes)

CPU Instruction Set
The M32R employs a RISC architecture, supporting a total of 100 discrete instructions.

(1) Load/store instructions
Perform data transfer between memory and registers.

LD	Load
LDB	Load byte
LDUB	Load unsigned byte
LDH	Load halfword
LDUH	Load unsigned halfword
LOCK	Load locked
ST	Store
STB	Store byte
STH	Store halfword
UNLOCK	Store unlocked

(2) Transfer instructions
Perform register to register transfer or register to immediate transfer.

LD24	Load 24-bit immediate
LDI	Load immediate
MV	Move register
MVFC	Move from control register
MVTC	Move to control register
SETH	Set high-order 16-bit

(3) Branch instructions
Used to change the program flow.

BC	Branch on C-bit
BEQ	Branch on equal
BEQZ	Branch on equal zero
BGEZ	Branch on greater than or equal zero
BGTZ	Branch on greater than zero
BL	Branch and link
BLEZ	Branch on less than or equal zero
BLTZ	Branch on less than zero
BNC	Branch on not C-bit
BNE	Branch on not equal
BNEZ	Branch on not equal zero
BRA	Branch
JL	Jump and link
JMP	Jump
NOP	No operation

(4) Arithmetic/logic instructions
Perform comparison, arithmetic/logic operation, multiplication/division, or shift between registers.

• Comparison

CMP	Compare
CMPI	Compare immediate
CMPU	Compare unsigned
CMPUI	Compare unsigned immediate

• Logical operation

AND	AND
AND3	AND 3-operand
NOT	Logical NOT
OR	OR
OR3	OR 3-operand
XOR	Exclusive OR
XOR3	Exclusive OR 3-operand

•Arithmetic operation

ADD	Add
ADD3	Add 3-operand
ADDI	Add immediate
ADDV	Add(with overflow checking)
ADDV3	Add 3-operand
ADDX	Add with carry
NEG	Negate
SUB	Subtract
SUBV	Subtract (with overflow checking)
SUBX	Subtract with borrow

•Multiplication/division

DIV	Divide
DIVU	Divide unsigned
MUL	Multiply
REM	Remainder
REMU	Remainder unsigned

•Shift

SLL	Shift left logical
SLL3	Shift left logical 3-operand
SLLI	Shift left logical immediate
SRA	Shift right arithmetic
SRA3	Shift right arithmetic 3-operand
SRAI	Shift right arithmetic immediate
SRL	Shift right logical
SRL3	Shift right logical 3-operand
SRLI	Shift right logical immediate

(5) Instructions for the DSP function
Perform 32-bit ×16-bit or 16-bit × 16-bit multiplication or multiply-Accumulate calculation. These instructions also perform rounding of the accumulator data or transfer between accumulator and general-purpose register.

MACHI	Multiply-accumulate high-order halfwords
MACLO	Multiply-accumulate low-order halfwords
MACWHI	Multiply-accumulate word and high-order halfword
MACWLO	Multiply-accumulate word and low-order halfword
MULHI	Multiply high-order halfwords
MULLO	Multiply low-order halfwords
MULWHI	Multiply word and high-order halfword
MULWLO	Multiply word and low-order halfword
MVFACHI	Move from accumulator high-order word
MVFACLO	Move from accumulator low-order word
MVFACMI	Move from accumulator middle-order word
MVTACHI	Move to accumulator high-order word
MVTACLO	Move to accumulator low-order word
RAC	Round accumulator
RACH	Round accumulator halfword

(6) EIT related instructions
Start trap or return from EIT processing.

RTE	Return from EIT
TRAP	Trap

(7) Instructions for the FPU function

The microcomputer supports fully IEEE-754 compliant, single-precision floating-point arithmetic.

FADD	Floating-point add
FSUB	Floating-point subtract
FMUL	Floating-point multiply
FDIV	Floating-point divide
FMADD	Floating-point multiply and add
FMSUB	Floating-point multiply and subtract
ITOF	Integer to float
UTOF	Unsigned to float
FTOI	Float to integer
FTOS	Float to short
FCMP	Floating-point compare
FCMPE	Floating-point compare with exception if unordered

(8) Extended instructions

STH	Store halfword(@R+ addressing added)
BSET	Bit set
BCLR	Bit clear
BTST	Bit test
SETPSW	Set PSW
CLRPSW	Clear PSW

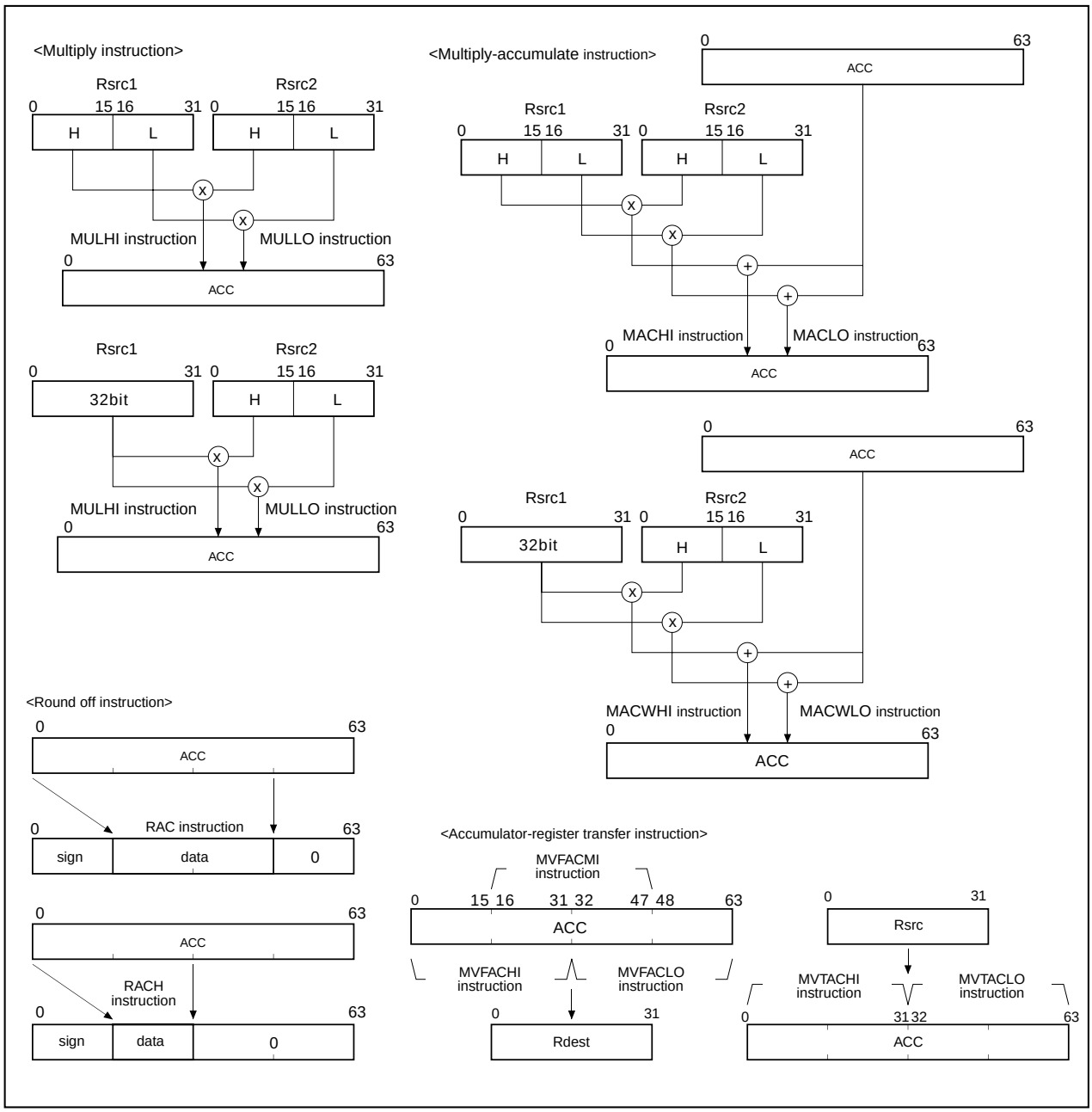


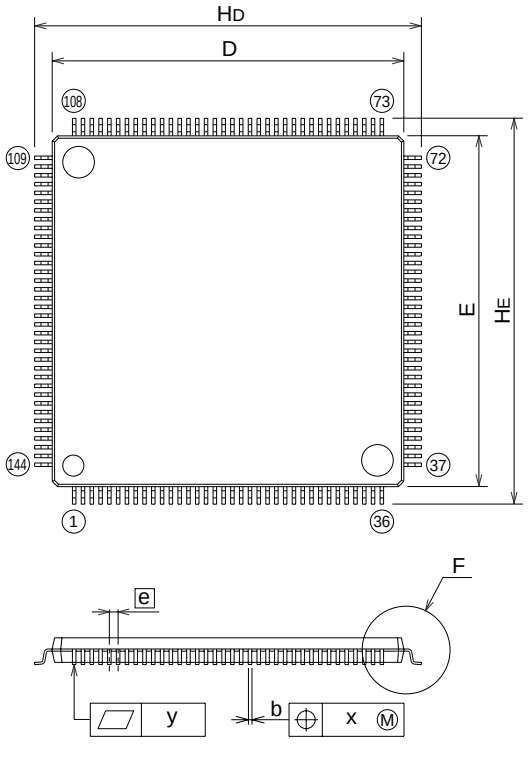
Figure 23. Instructions for the DSP Function

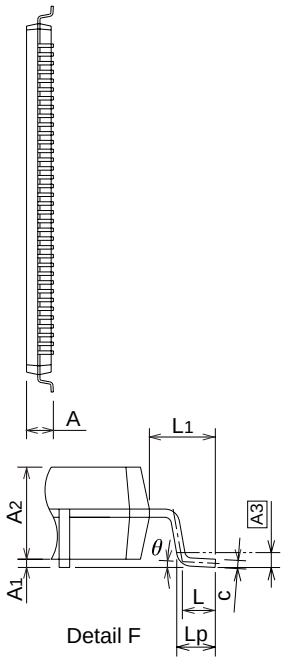
Package Dimensions Diagram

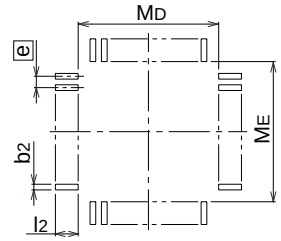
144P6Q-A (MMP)

Plastic 144pin 20 × 20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy







Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	0.95	–	–
MD	–	20.4	–
ME	–	20.4	–

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RENESAS
Renesas Technology Corp.

REVISION HISTORY	32182 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.0	07/12/02	-	First Edition.
1.2	10/11/02	Entire page	Add 1024KB version of Flash Memory product to line-up.