

LKT4200HS

32-BIT ENCRYPTION MICROCONTROLLER

DATA SHEET

Revision 4.1

深圳市春东电子有限公司
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Data Sheet, Revision V4.1

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1. Features

CPU

- SC100 32-bit CPU core
- Fully 16/32-bit RISC architecture
- CPU internal frequency: up to 84Mhz

Memory Allocation

- 64KBytes for user data area
- 16KBytes for NVM data area
- 4K-Byte static RAM
- Memory Protection Unit (MPU) support 1GB

Flash Operations

- Min. 100,000 erase/write cycles
- Min. 10 years data retention

Data Security

- 256-byte security (Read-only) and 256-byte nonerasable flash area
- Abnormal condition detectors for reset operation: voltage, frequency, temperature, light, glitch, inner insulation layer removal or active shield layer removal
- Dynamic RAM data encryption
- Security optimized layout

MPU (Memory Protection Unit)

- Individual protection attributes up to 8 separate regions
- Each region can start and end on any 64-byte boundary
- Support up to 1GB of memory space
- Alignment, overflow, and region permission Protection

DES/T-DES

- Built-in hardware DES/TDES
- Adoption of virtual DES system for security
- Dummy logic for DES operation

Serial I/O Interface (UART)

- Asynchronous half-duplex serial interface which conforms to ISO 7816-3
- One hardware UART supporting T=0 and T=1

Parity/CRC calculator

- Parity calculator for 8/16/32 bit
- CRC-16/32 calculator

Timers

- Two 16-bit programmable interval timers
- One 20-bit watchdog timer

Random Number Generator

- 16-bit random number generator

Clock Controller

- External Clock
- Internal RC clock

Reset

- Power-on reset and external reset
- Power-on reset flag

Operating Characteristics

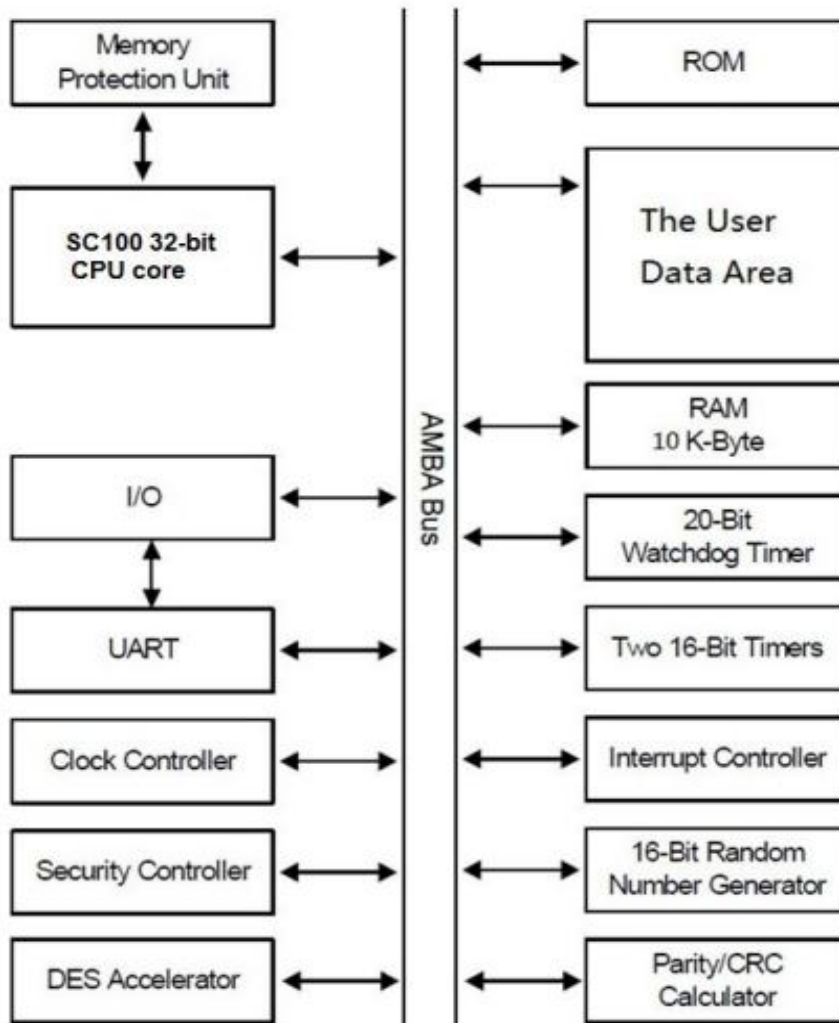
- Single power supply: 1.62 ~ 5.5 V
- Operating frequency: 1 to 10 MHz (External clock @class A/B.)
- Operating temperature: - 25°C to + 85 °C

Operating Current

- Max. 10mA (Vdd = 5.5V, Fclk = 5MHz)
- Max. 6mA (Vdd = 3.3V, Fclk = 4MHz)
- Max. 4mA (Vdd = 1.98V, Fclk = 4MHz)

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2. Block Diagram

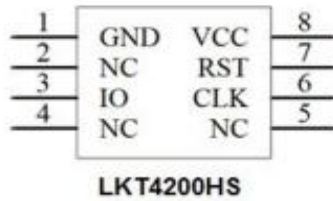


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3. Pin Assignments

Table 1. LKT4200HS Pin Descriptions

Pin Number	Pin Name	Function Description	Pin Type
1	GND	Ground	---
2	NC	No connection	---
3	I/O	Serial data input and output pin	Input/output
4	NC	No connection	---
5	NC	No connection	---
6	CLK	External clock input	input
7	RST	System reset input	input
8	Vcc	Power input	----

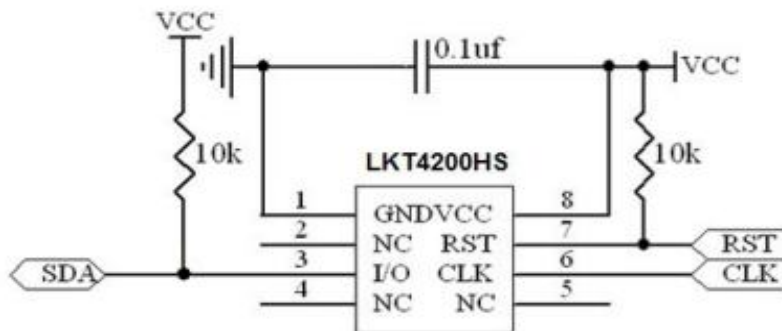


Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD1}	$f_{CLK} = 5 \text{ MHz}, 5.5 \text{ V}$	–	–	10	mA
		$f_{CLK} = 4 \text{ MHz}, 3.3 \text{ V}$	–	–	6	
		$f_{CLK} = 4 \text{ MHz}, 1.98 \text{ V}$	–	–	4	
Stop Current	I_{DD2}	$f_{CLK} = 1 \text{ MHz}, 5.5 \text{ V}$	–	–	200	uA
	I_{DD3}	$f_{CLK} = \text{GND}, 5.5 \text{ V}$	–	–	100	
Cell erase cycle time	T_{EC1}	Page	–	0.3	–	ms
	T_{EC2}	Sector	–	1.5	–	
	T_{EC3}	Bank (Chip)	–	3.0	–	
Cell write cycle time per 32 WU (32 word)	T_{WC}	–1	–	0.3	–	ms

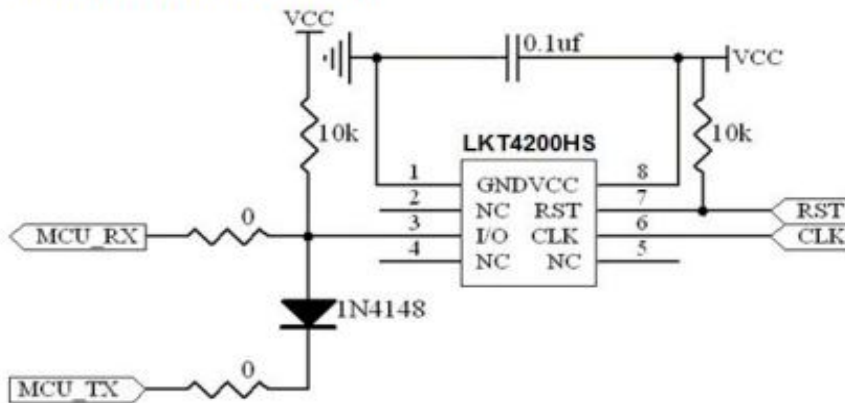
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4. Typical Application Circuits

A. I/O simulation uart serial communication



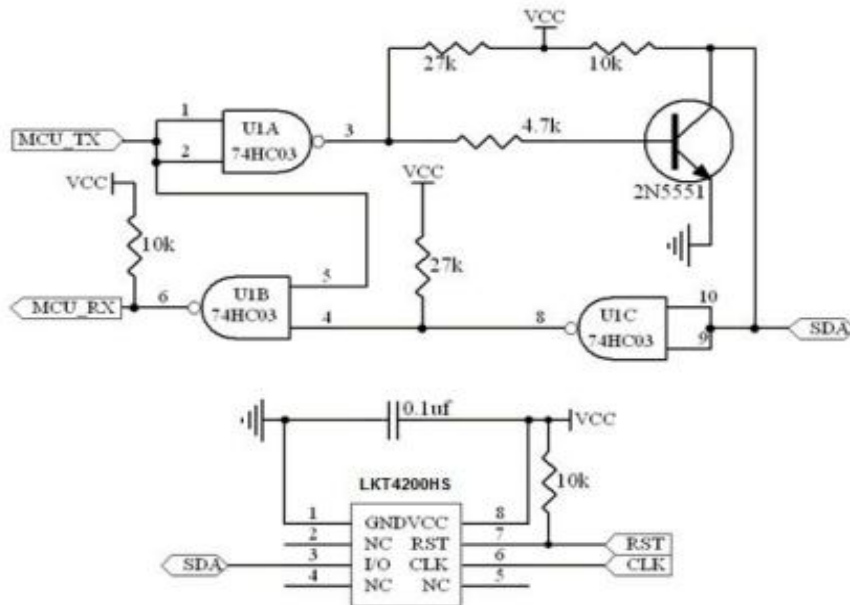
B. Using the uart interface (Simplify)



Use uart simplify the circuit, the MCU TX send data at the same time the MCU RX to prohibit the receive data, the purpose is to prevent the MCU receives a useless redundant data

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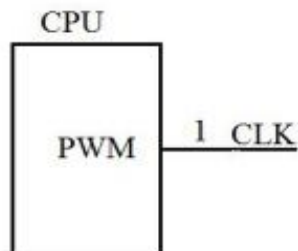
C. Using the uart interface



D. The following three ways to use CLK

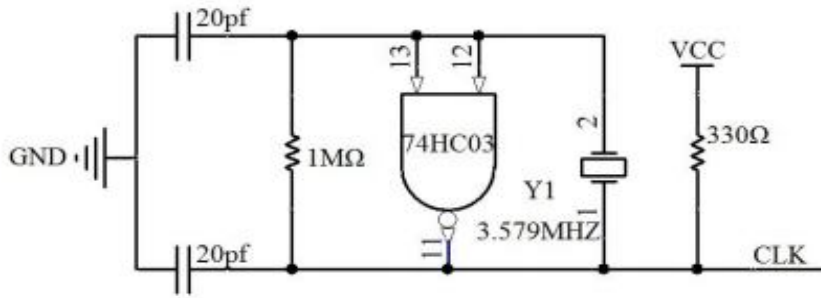
If the PWM wave client for CPU can provide CLK clock, recommends that customers use PWM wave that can save the cost.

(1) PWM wave CPU users to provide the CLK clock.

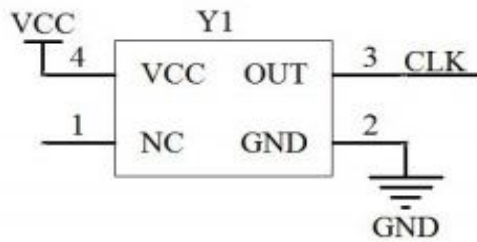


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(2) Passive crystal and a peripheral circuit provides CLK clock. Y1 is equal to 3.579MHZ just as an example.



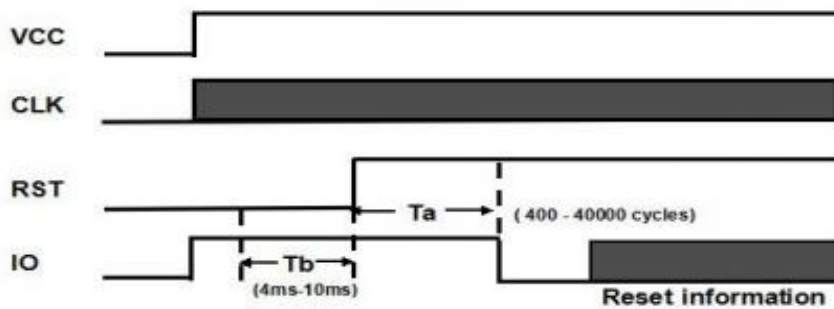
(3) Active crystal directly provides CLK clock.



5. Communication debugging

A. Reset Timing

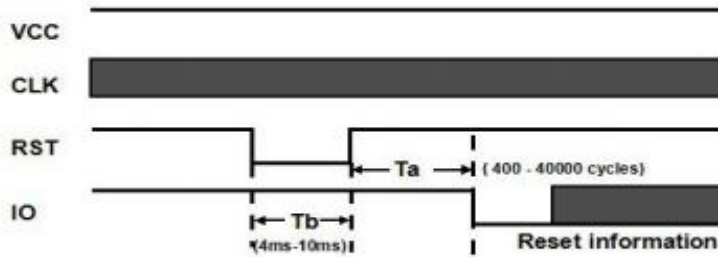
Cold reset



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I/O waiting for the start signal is high. When the RST pin goes high, the chip T_a (400-40000 cycles) times after the reset information.

Hot reset



I/O waiting for the start signal is high. When the RST pin low to high, the chip T_a (400-40000 cycles) times after the reset information.

Clock signal requirements

B. CLK



1. LKT4200HS need to be Provide 1M to 10M CLK
2. The duty cycle is about 40%~60%.

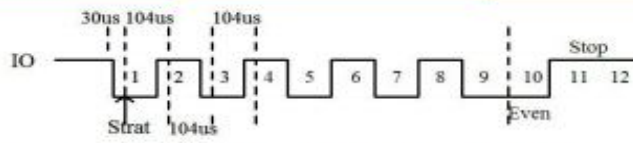
C. I/O simulation uart serial communication Timing

LKT4200HS use 1 start bit 8 data bits, even parity, 2 stop bits uart serial communication.

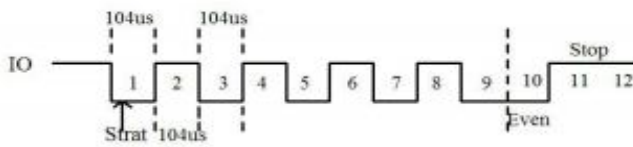
Receive timing

The timing diagram: The timing diagram in order to use the crystal 3.579MHZ, receive data for the 0x55 as an example. The first start bit, 2-9 for data bits, 10 for even parity bits, 11-12 for two stop bits. System power-up default communication baud rate ($F_{osc} / 372$) 3.579MHZ when the default baud rate is 9600. I/O simulation UART communication concern is 9600 baud per a data retention time is etu. By calculating ($372 / 3.579$) 9600 baud, each data retention time is about 104us.

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In order to ensure receiving data stability .after receipt of the start bit 130us after every 104us receive next bits.

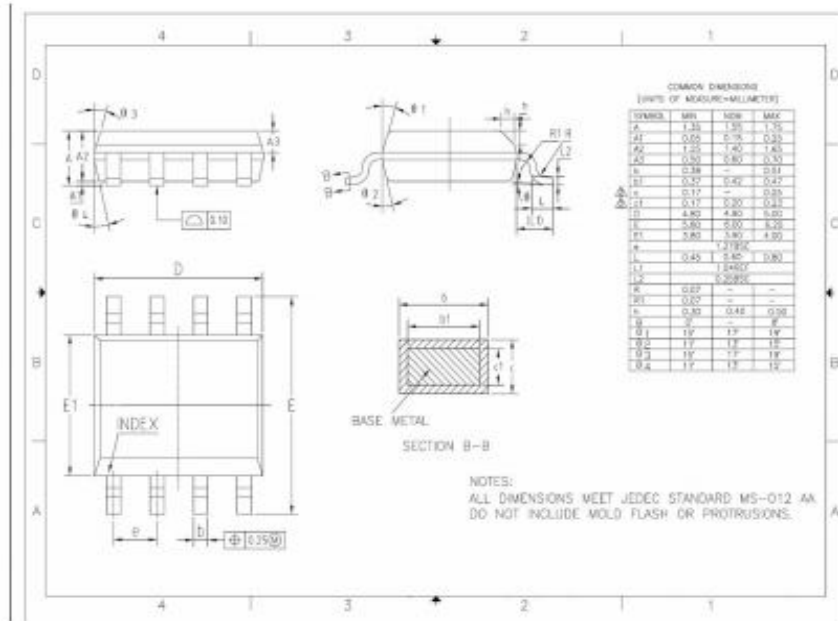


Send timing

Send timing stringent than the receiver timing point each time to send one to keep in a etu.

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6.LKT4200HS sop8 package specification



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